VITA News

By Ray Alderman

Is it time for a new mezzanine card standard?

Any discussion about mezzanine cards requires a recap of some industry history. Back in 1990, there were more than 50 mezzanine specifications in the market. That was problematic. The PMC specifications started with the Institute of Electrical and Electronic Engineers (IEEE), with the S-bus electricals from Sun Microsystems. That migrated to using PCI electricals when PCIbus was announced. Additionally, pinouts were added to support processors, PrPMC. When the high-speed differential-serial fabrics were announced, another connector was added to the PMC specification called *XMC* (Switched-serial Mezzanine Card).

Even with this history, we need to start thinking about a new mezzanine standard for the embedded markets. A discussion of mezzanines also requires a review of the markets. The primary users of mezzanine cards include the military and industrial markets. The military market requires a number of different interfaces such as 1553, Fibre Channel, and others on its CPU cards, and it needs the flexibility a mezzanine card offers. Putting certain functions on mezzanine cards also offers the MIL/COTS users a reasonable strategy for chip obsolescence: They can replace the obsolete chip with a new one on a new mezzanine. The industrial markets have even more interfaces to deal with (TTL I/O, opto-isolated I/O lines, A/D and D/A interfaces, motor controllers, and others). Telecoms seem to use mezzanine cards for prototyping and systems development, since they have only a few interfaces required. When a telecom company has the basic configuration completed, tested, and the software written, they expect their board supplier to consolidate the functions from the mezzanine card hard-down onto the CPU card and reduce the cost of the board and the system.

Today, we have other mezzanine efforts underway at VITA besides the basic high-speed serial V-42 XMC efforts. We have an FPGA mezzanine standard under development (V-57), and with the Aurora protocol standard for mezzanines (V-55). We have seen interest in the HyperTransport Mezzanine specification (V-42.4) and in the front-panel insertable mezzanine card (V-56), as well as the live-insertable mezzanine card (V-43S). It is clear that there are a number of applications for mezzanine cards for new and different purposes.

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Without getting into the PMC/PrPMC/XMC shortcomings, we need to think about a new unified mezzanine specification. The frequencies of the serial fabrics are all moving from 2.5 GHz to 5 GHz, and then to 10 GHz and above. Present mezzanine connectors may not handle the next level of frequencies. Concurrently, the PCI bus is rapidly heading toward end of life. Empirical evidence of this increased frequency trend in 2007 indicates the sales of basic 2.5/3.125 GHz connectors declined, and sales of 5-6-10 GHz connectors increased dramatically, according to the latest Bishop & Associates reports. So, it is evident that the 2.5/3.125 GHz silicon (and the supporting connectors) could have a very short life cycle.

Today, we are seeing the need for new mezzanine cards for specific applications such as FPGA-based computing, flash memory mass storage, higher-performance processor chips, and Software-Defined Radios. In my opinion, the present set of PMC/XMC specifications just will not be able to handle these needs. We need to move up to a larger mezzanine card size, accommodate the higher signal frequencies, adapt the boards for conduction- and liquid-cooling capabilities, and handle the changing power supply voltages of the newer chips.

I have stated my ideas for an eight-sided mezzanine card many times. The eight sides of such a card are at 45-degree angles. The power connector is always at the bottom of the card at 180 degrees. The front-panel I/O connector is always at 0/360 degrees. If the card is an I/O mezzanine card, the additional signal connector is placed on the plus 45-degree side. If it is a Processor Mezzanine Card, the connector is placed at plus 90 degrees from zero. If it is a mass storage memory card, the connector is placed at plus 135 degrees from zero. This would completely eliminate any kinky keying mechanism and guarantee that the wrong type of card could never be plugged into the wrong sockets on the baseboard. We still have more connector positions left for other types of mezzanine definitions (such as FPGAs, DSPs, SDR, graphics, and others). And, we don't have to mix power pins and signal pins in the same connector body as we presently do with the PMC/XMC specification.

You may not agree with my eight-sided mezzanine card idea. But you have to agree that it is time to start thinking about what the next-generation mezzanine card needs to accommodate, and what it needs to resemble. Before we know it, the demand for a new card format for industrial and military markets will be upon us. We need to anticipate how we are going to design it and build it for critical systems. I just do not see telecoms using mezzanines in volume. They seem to follow the old workstation market model, everything goes hard-down on the motherboard. They do not need the flexibility required by the industrial or military markets.

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