

# 2eSST: Today's VME performance booster

By Subhankar Bhattacharya and Leif Erik Laerum

VME deployment has grown increasingly since its adoption in the early 1980s, renewing and evolving as newer and better technologies are added to its architecture. During the past 25 years, VME has kept pace with innovation by increasing data transfer rates, adding fabric connectivity while maintaining backward compatibility at the pin level to preserve legacy functionality and investment. VME has reigned in critical embedded applications because it provides the required level of determinism, low latency, and low processing overhead. Now 2eSST moves to the front lines, accelerating VMEbus performance.

High-end, critical embedded systems using I/O-intensive applications – such as data recording, industrial control, and sensor I/O – use multiple processors, distributed memory, and several I/O cards, requiring large backplane bandwidth. In addition, as processors continue to augment performance and memory increases in size, at some point the backplane bus becomes a bottleneck. In some applications, this has already happened to the VME64 bus. It is no longer being designed as the data path but is used as a control plane for housekeeping and management. In this case, a designer has two choices for improving card data rates:

- Choose a hybrid backplane as detailed in VITA 41 (VXS) and/or VITA 46 (VPX) in which a serial bus is added in conjunction with the VMEbus. With this choice, designers have to adopt one of the serial-based interconnect technologies such as RapidIO, GbE, or PCI Express.
- Increase the VMEbus speed with a VME protocol such as VME320 (2eSST).

In addition to considering higher data rates, designers also need to consider the ease of implementation, the preservation of legacy functionality, and costs in their design choice. If the designer chooses a VXS or VPX backplane, the addition of a serial bus is a much larger undertaking than increasing the VMEbus throughput. This option requires investment in a new backplane, new software, new architecture, and new test gear. This is in addition to the challenge of creating, verifying, and troubleshooting a robust, deterministic interconnect between the distributed compute elements.

On the other hand, designers can still increase VMEbus performance by a factor

of 10 without major adjustments in software and hardware when using the 2eSST protocol. There are many VME cards that support these newer protocols available today. Even if the designer sees a need to eventually implement a serial bus for high-speed data plane traffic, there may be a simultaneous need for increased VMEbus speed to deal with increased local or control plane traffic.

### 2eSST boosts performance

Introduced in 1997, 2eSST stands for *Two Edge Source Synchronous Transfer* and complies with ANSI/VITA 1.5-2003. It is a high-performing VME standard, increasing the data rate transfer over the tried-and-true DIN connector by an order of magnitude. 2eSST provides a significant performance improvement level and can achieve sustained data transfer rates up to 320 MBps in a full chassis of up to 21 cards. Equivalent to a 2.5 GBps increase or representing more than an 8x improvement over conventional VME32, 2eSST enhances the VMEbus' ability to enable new high-performance applications.

Traditional VME data transactions perform single cycle transfers of 32 data bits

with a maximum transfer rate of 40 MBps. Multiplexed Block Line Transfer (MBLT) in the VME64 standard uses 32 data lines and 31 address lines plus LWORD to create a 64-bit bus and a transfer rate of 80 MBps. With 2eSST, the transmitter does not wait for acknowledgement (DTACK\*) from the receiver before sending the next byte of data. This means that bandwidth is limited not by the time of flight (send, receive, send acknowledgement back) but by skew between the data signal lines.

Another useful feature implemented in 2eSST is broadcast transfers. These permit sending data to all the slaves on the bus in one transaction instead of 20 repeated transmissions. Designs built to the VITA 1.5-2003 standard will support rates up to 320 MBps in a 21-card backplane implementation. This is an improvement of 3x over GbE rates. In addition, 2eSST has lower latency and higher determinism and uses significantly less CPU bandwidth than GbE. A closer look at the timing diagrams will show how VME64, 2eVME, and 2eSST function.

Figure 1 illustrates that the main difference between 2e and VME64 is that data

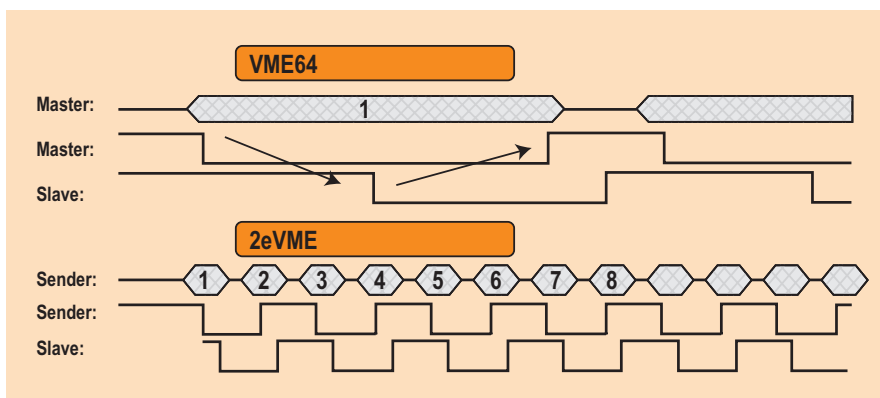


Figure 1

is latched on both edges (2e). In Figure 2, which shows a 2eSST transaction, we see that a 2eSST master does not wait for handshaking from the slave, whereas 2eVME does. Cursor T is set to the point where the address is valid. This is the very beginning of the transaction. DTACK then toggles three times (three edges). There is one edge for each address phase. There are additional attributes communicated to the slave during these phases. Then DTACK stays low after that during the data phases. DTACK is asserted by the slave. The master toggles DS1. A new data value is latched by the slave for each edge on DS1. Cursors X, Y, and Z show the speed of the data. In this case, a new data value is received every 30 ns.

It is also worth noting that the specification calls for backwards compatibility. So if there are VME endpoints on the bus that are functioning at VME64 speeds, the endpoints supporting 2eSST are *not* throttled back. This means that as long as there are two or more cards employing the 2eSST standard, performance gains will be realized.

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**Designers now have more choice**  
Today’s designers have the diagnostic tools, bridge products, and backplane design knowledge required to build 2eSST systems. VME cards using 2eSST are now available and include products from companies such as Curtiss-Wright, GE Fanuc, Motorola, Tundra Semiconductor, and VMETRO. The Tundra Tsi148 PCI-X-to-VME bridge and the VMETRO Vanguard VME analyzer are examples of products supporting both 2eSST and 2eVME pro-

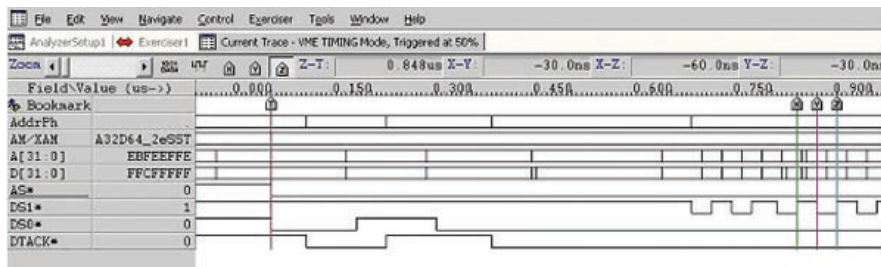


Figure 2

VME Slave Accesses (AS assertion to DTACK negation on VMEbus)		
Packet Size & Transaction	2eSST-enabled Bridge	Legacy VME Bridge
2 KB Write	313 MBps	108 MBps
2 KB Read	301 MBps	101 MBps
32-bit SCT Write (total 4 bytes)	62 MBps	29 MBps
32-bit SCT Read (total 4 bytes)	18.6 MBps	14.2 MBps
PCI Target Access (Frame assertion to TRDY negation)		
Packet Size & Transaction	2eSST-enabled Bridge	Legacy VME Bridge
4 KB Burst PCI Write	1,061 MBps	75 MBps
4 KB Burst PCI Read	277 MBps	11.4 MBps
DMA Performance (Values are highly dependent on application)		
Packet Size & Transaction	2eSST-enabled Bridge	Legacy VME Bridge
8 KB DMA PCI to VME	234 MBps	80 MBps
8 KB DMA VME to PCI	55 MBps	249 MBps

Table 1

ocols that can create high-performance VME products now.

**The proof is in the test results**

Just how much better would performance be using 2eSST-supported devices? Performance benchmarking against a legacy bridge chip demonstrates the performance gains possible in a 2eSST system. Table 1 highlights the benchmark results for VME slave accesses, PCI target access, and DMA performance successively. Please note: multiple types of transactions and packet sizes were used in this benchmark.

**2eSST – Extending the life expectancy of the VMEbus**

VME has continued to succeed not just because it is an open standard but because it also promotes backwards compatibility, has a large ecosystem, and has continued to evolve over time. VME has embraced

continuous evolution and introduced new protocols to keep pace with the improvements in microprocessor and communications technology. The addition of 2eSST further extends VMEbus’ position as the backplane bus of choice in critical embedded systems for many years to come. Maintaining the promise of lower latency and determinism, in addition to faster data transfer rates, makes 2eSST a compelling solution to upgrade performance. 2eSST can dramatically boost VMEbus performance without significant change to system architecture. 2eSST also provides a persuasive argument for designers to think twice about the premature and costly step of implementing a hybrid serial VME backplane to increase their VME performance. Although that may be a viable option, the 2eSST solution should be explored first. **CS**



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