Serial fabrics boost Software-Defined Radio system performance

By Rodger Hosking

Moving data within a high-performance Software-Defined Radio system can be a challenge when using traditional architectures dependent on buses and parallel connections. New methods for remedying the problem leverage FPGAs, gigabit serial links, and switched fabric standards.

The most difficult problem for designers of high-performance, Software-Defined Radio systems is simply moving data within the system because of data throughput limitations. Traditional system architectures relying on buses and parallel connections between system boards and mezzanines fall far short of delivering the required peak rates and suffer even worse if they must be shared and arbitrated. New strategies for solving these problems exploit FPGAs, gigabit serial links, and switched fabric standards to create significantly more powerful architectures ideally suited for embedded Software-Defined Radio systems.

Gigabit serial fabric defined

The descriptive phrase "gigabit serial" covers a truly diverse range of implementations and application spaces. Figure 1 shows most of the popular standards used in embedded systems suitable for Software-Defined Radio, along with how each standard is typically deployed in a system.

All of these standards are endowed with numerous subspecifications that define the physical layer, the cable medium, data rates, and system topologies. The venerable Ethernet heads the list as the ubiquitous networking link, originally operating at 10 MHz rates, but now commonly running at 1 GHz (1 GbE). Next-generation 10 GHz devices are already appearing with 100 GHz not far behind.

Within the past decade, high-performance hard disk drives for real-time data storage shifted from parallel SCSI interfaces to serial Fibre Channel links running at 1 or 2 GHz, over both copper and optical cable. Now 4 GHz rate interfaces and drives are becoming common, delivering peak data rates of up to 400 MBps.

PCI Express (PCIe) evolved to replace the parallel PCI bus for motherboard peripherals and expansion slots in personal computers. Current data speeds of 2.5 GHz will be extended to 5 and 10 GHz as the supporting technology evolves. Since PCIe delivers only point-to-point interconnects, a routable derivative protocol called *Advanced Switching Interconnect* is being developed to encourage simultaneous data flow from one source to another.

Standard	Main application
GbE	Computer networking
Fibre Channel	Data storage
PCI Express	Peripheral interconnect
Serial RapidIO	System interconnect
Aurora	Streaming data
Serial ATA	Data storage
InfiniBand	System interconnect
HyperTransport	Peripheral interconnect

Figure 1

Serial RapidIO emerged as a solution targeted for interconnecting components and boards in real-time embedded systems. Unlike some of the other standards, Serial RapidIO offers low latency and deterministic behavior, essential in applications like Software-Defined Radio.

Aurora is a link-layer protocol developed by Xilinx to support efficient point-to-point serial connectivity for streaming data between FPGAs. In Software-Defined Radio applications, Aurora is ideally suited for raw data streams from A/D converters requiring maximum throughput with low overhead and an extremely lightweight protocol.

FPGA technology support

Following the advancing trend toward gigabit serial interconnects, Xilinx and Altera have incorporated increasing support features in their recent device families. Figure 2 shows the evolving gigabit serial features of the Xilinx FPGAs. As you can see, the Xilinx Virtex-II Pro was the first device to offer RocketIO gigabit serial transceivers.

The FPGA devices include the low-level electrical interface, the SERDES (serializer and deserializer), and 8B/10B encoding engine that delivers clock and data over a single differential pair of copper lines. This interface constitutes the underlying physical and transport layers common to most of the popular gigabit serial standards, including Aurora, PCI Express, Serial RapidIO, InfiniBand, and HyperTransport.

	Virtex-II Pro XC2VP50	Virtex-4 XC4VFX100	Virtex-5 XC5VLX220T
Logic Cells	53,136	94,896	221,184
Block RAM (bits)	4,176 k	6,768 k	7,632
Max I/O User Pins	852	768	680
Multipliers	232	160	128
405 PowerPCs	2	2	-
RocketIO Serial	**16**	20	16
GbE ports	-	**4**	4
PCI Express ports	-	-	**1**

Figure 2

Protocol engines for specific standards can be configured using FPGA logic so that FPGAs can adapt to different protocols as required. They interface to the SERDES and correctly process protocol-specific packets, header information, control functions, error detection, and correction and payload data format. The strategy makes FPGA-based XMC modules truly "fabric agnostic" and allows one hardware design to be deployed in several different fabric environments.

This flexibility in using one hardware product to cover several different protocols encourages board vendors to develop FPGA-based products for the general market. It also affords system integrators the luxury of not having to commit to any particular standard when selecting boards for their systems. This saves the integrator valuable time and money by offering the flexibility of choosing the fabric that works best for their particular application.

Since gigabit serial interfaces on FPGAs were so well received in the embedded computing market, FPGA vendors took the next step and added additional levels of integration to support the most popular gigabit serial protocol: GbE. The Xilinx Virtex-4 incorporates four 1 GbE MACs connected to RocketIO electrical transceivers. These MACs offload a significant amount of low-level protocol processing to save FPGA resources for more worthy tasks such as IP core installation.

In their latest Virtex-5 family, Xilinx offers their RocketIO GTP transceivers with bit rates up to 3.125 GHz. Altera offers their Stratix-II GX multigigabit transceivers with bit rates up to 6.375 GHz.

The new Xilinx Virtex-5 LXT devices advance the technology even further by including a built-in PCI Express endpoint engine. For example, having this feature built in saves approximately 18,000 logic cells, which equates to 59 percent of the total logic cells available on the Virtex-5 LX30T that can be used for other tasks.

Embedded system switched fabric standards

Standardization of gigabit serial fabric protocols and silicon devices with available interfaces fostered the development of standards suitable for deploying them in real-time embedded systems for Software-Defined Radio. These include the XMC switched fabric for PMC and VXS switched fabric for VMEbus.

XMC – Switched fabric for PMC

The hallmark of any successful standard is that it continues to evolve with technology, and none offers a better example than XMC. The VITA 42.0 base specification includes general information, reference and inheritance documentation, dimensional specifications, connectors, pin numbering, and primary allocation of pairing and grouping of pin functions. The VITA 42.0 base specification does not dictate signal types, data rates, protocols, voltage levels, or grouping for these signals. Instead, it wisely leaves that up to the several subspecifications that follow, allowing XMCs to evolve as new standards emerge.

XMCs can be single- or double-wide modules that use high-performance connectors with full-duplex gigabit serial differential pairs. A single-width XMC can have one or two connectors, while a double-width XMC can have up to four connectors. Each connector can support data transfer rates up to 2.5 GBps using 3.125 GHz bit rate signals.

XMC modules can be installed on a wide range of carrier boards including VME, VPX, CompactPCI, and PCI. The clear benefit here is that by following these definitions, XMC and carrier board designers can achieve a much wider range of interoperability, the essential goal of industry standards.

VXS – Switched fabric for VMEbus

VXS, defined under the VITA 41 specification, is fully backwards compatible with VME64x and incorporates a new seven-row MultiGig RT2 connector that sits between the P1 and P2 connectors at the backplane interface that accommodates two VXS links. Each VXS link operates in a full duplex mode for simultaneous transfers in each direction, and gangs four serial lines together to increase speed. Serial bit rates are defined for frequencies up to maximum of 10 gbps, although lower frequencies are supported for initial systems. With the 4x ganging and a nominal bit frequency of 3.125 GHz, both input and output paths for dual 4x links are capable of moving data between system cards at 2.5 GBps.

Many VXS-based systems designate the VMEbus as a control plane with all high-speed transfers moving across gigabit links. The VITA 41.6 specification seeks to replace this control plane function with a separate GbE port using extra pins defined on the RT2 connector. This concept extends well into some versions of the next-generation architecture, VITA 46 or VPX, which replaces the VMEbus connectors with additional gigabit serial connectors for even higher board-to-board connectivity.

VXS processor SDR example for XMC modules

Figure 3 shows a simplified block diagram of Pentek's Model 4207 VXS processor

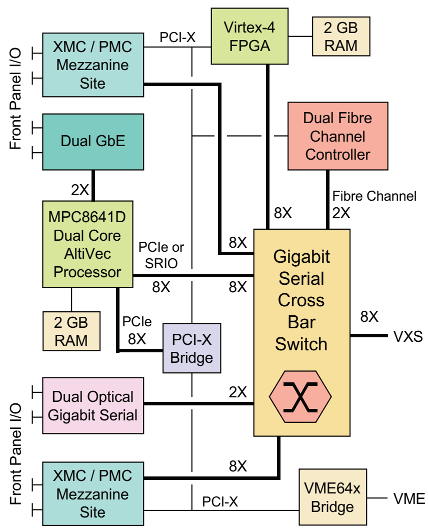

Figure 3

board, which utilizes gigabit serial technology for interconnecting every major board resource. Perhaps the most significant resource on the board is the fabric-transparent crossbar switch. Because all high-speed interfaces on the board connect through the switch, paths can be configured to meet specific requirements. For example, XMC modules can transfer data through the switch to the onboard FPGA, to the processor, to the other XMC, or to another board over the VXS connector. Similar types of connections are available for other resources, using any protocol that the connected devices support, including Serial RapidIO, PCI Express, InfiniBand, and Xilinx Aurora protocols. The board thereby provides accelerated power, speed, and connectivity in a single slot, making it well suited for wideband, data acquisition and recording, real-time DSP, and Software-Defined Radio applications.

By installing two Model 7140 PMC/XMC Software-Defined Radio transceiver modules, see Figure 4, on the Model 4207 processor board, a complete four-channel Software-Defined Radio transceiver system is created. Data in and out of the four A/Ds and four D/As can be routed through the MPC8641D processor, through the FX60 FPGA, through the Fibre Channel interface to hard disk, or through the VXS backplane port. Each scenario is achieved by appropriately configuring the crossbar switch to enable the desired paths. Since the processor controls the crossbar switch, the signal flow architecture can be changed during runtime to track application requirements.

Gigabit interfaces provide high performance

With each new generation of powerful, high-performance embedded solutions – including processors with higher clock rates and wider buses, data converter products with higher sampling rates, and FPGAs and DSPs offering incredible computational rates – there must be an equally powerful solution to keep up with the data transfer rates and eliminate system bottlenecks. Gigabit serial links can dramatically improve Software-Defined Radio applications' performance in ways that were unattainable with earlier technology. **CS**

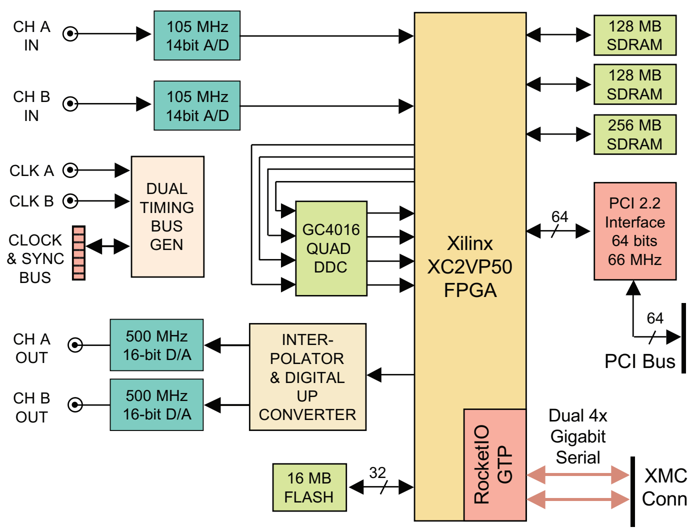

Figure 4

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