



The VME Renaissance constitutes a period of increased intellectual activity and technology insertion surrounding the VMEbus over the next few years, an epoch of innovation and performance improvement that maintains backward compatibility and protects legacy customer investments. Motorola announced the inception of the VME Renaissance at the Bus & Boards Show in January 2002. Since that time, there have been a number of important milestones and announcements regarding the VME Renaissance.

The Tempe ASIC

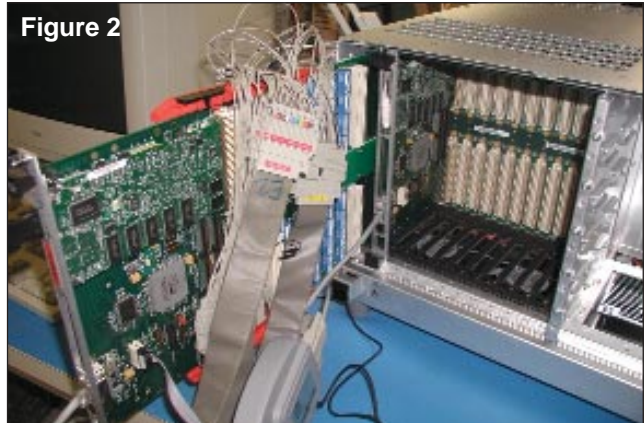
One of the first significant events in the VME Renaissance was the January announcement of Motorola's development of the PCI-X-to-VME Bridge ASIC code named "Tempe" (see Figure 1). Tempe will be the first bridge to support both a 133 MHz PCI-X bus and a 2eSST-capable VMEbus interface. Utilizing this device, users will be able to simultaneously maximize both VMEbus and PCI bus performance. A more detailed description of the Tempe ASIC can be found in the February 2002 issue of *VMEbus Systems* magazine.



The design of the Tempe ASIC by Motorola has progressed well since it was first announced in January. Motorola anticipates transitioning the design to sample manufacturing in December 2002. Currently, the design team is in the process of testing the design using both simulation tools and actual proof-of-concept boards, each populated with the TI SN74VMEH22501 VMEbus transceivers and an FPGA that implements the Tempe ASIC's internal logic. These proof-of-concept boards are currently communicating with each other across a standard VMEbus backplane using the 2eSST protocol. The actual test platform and proof-of-concept boards are shown in Figure 2.

In August 2002, Motorola and Tundra Semiconductor announced an agreement where Tundra will market, manufacture, sell, and support the Tempe ASIC. In addition to these responsibilities, Tundra will also provide future enhancements to the product. Motorola also reaffirmed its intention to develop products based on the Tempe ASIC. This important announcement paves the way for all members of the VMEbus community to implement state-of-the-art VMEbus designs using the Tempe chip.

Figure 2



2eSST transceivers

Prior to the VME Renaissance, the 2eSST protocol was not supported on standard VMEbus backplanes. In order to achieve 2eSST speeds across a standard VMEbus backplane, a new type of VMEbus transceiver chip was required. An important milestone in the VME Renaissance was achieved in April, when Texas Instruments announced the availability of a transceiver that utilizes incident wave switching technology. Motorola and the VITA 2.1 Working Group worked with TI to develop and test the transceiver. An article describing Motorola's test results can be found in the August 2002 issue of *VMEbus Systems* magazine. Utilizing the Tempe ASIC together with the TI transceivers, products can be created that achieve 2eSST speeds in existing VMEbus backplanes.

New VMEbus board products

The early stages of the VME Renaissance have been marked by a trend of significant increases in both processor and I/O performance. Motorola has just announced the first board-level product that is part of that trend, the MVME5500 single board computer. The MVME5500 utilizes an MPC7455 processor with AltiVec technology, running at 1+ GHz, to provide users with outstanding vector, floating point, and general-purpose computing performance. Additional performance increases embodied in the MVME5500 include a 133 MHz processor bus, 2 Mbytes of L3 cache running at 266 MHz, dual 64-bit/66 MHz PCI buses with a PMC slot residing on each bus, a Gigabit Ethernet port, and up to 2 Gbytes of PC133 memory.

The VXS (VME Switched Serial) standard

While the above milestones represent evolutionary events in the VME Renaissance, the VXS Standard will bring a revolutionary change to the VMEbus ecosystem. This change promises to extend the life of the VMEbus for at least another decade.

In December 2001, the Motorola Computer Group (MCG) began working to define a data plane interconnect within the VMEbus ecosystem using standard switched serial topologies. A set of proposals named VXS were generated with the goal of creating a flexible framework to accommodate a number of switched serial protocols such as InfiniBand, Serial RapidIO, 10 Gigabit Ethernet, Fibre Channel, and PCI Express (also known as 3GIO).

The VXS Special Interest Group (SIG) was formed in January 2002 by MCG and included representatives from Sky Computers, Mercury Computer Systems, Tyco Electronics, Schroff-Pentair, and Mitre. The main goal of the VXS SIG was to add a switched serial interconnect to VMEbus coincident with the VME parallel bus using standard open link technologies. Additional goals were to maintain backward compatibility within the VMEbus ecosystem and provide more power to each VMEbus card.

Each of the VXS SIG members made significant contributions in preparing the proposals for presentation to the VITA Standards Organization (VSO) in March 2002. Immediately following the presentation of the proposals, the VXS Working Group, VITA 41, was formed in the VSO. The three draft proposals that were adopted by the VXS Working Group include:

- The VXS.0 Base Proposal, which details the physical features required to provide high-speed interconnects within a VME system.
- The VXS.1 InfiniBand Protocol Layer Proposal, which is built upon VXS.0 and describes how VXS boards interconnect and communicate using the InfiniBand protocol. It also defines the mechanical dimensions, pin assignments, and keying for the payload and switchboards.

- The VXS.2 Serial RapidIO Protocol Layer Proposal, which is very similar to VXS.1, except it implements Serial RapidIO instead of InfiniBand for the protocol layer.

An additional proposal, VXS.10, was generated about two months later to describe how to implement live-insertion (or hot-swap) in a VXS system.

All of these proposals have gone to ballot and are expected to be ratified as draft standards in September 2002. When they are ratified, it is expected that several companies will initiate development of VXS systems.

Summary

It should be evident by now that the VME Renaissance has been progressing at a rapid pace. From the time it was first announced in January 2002 until now, great strides have been made and many more are on the horizon as the VME Renaissance continues to unfold.



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