

The successful implementation of the VME 2eSST protocol in non-proprietary backplanes is another important milestone that has been reached as the VME Renaissance continues to unfold. Preliminary test results indicate that Texas Instruments' new VMEbus transceiver can be used to successfully implement the 2eSST protocol on standard VME64x 5-row backplanes. This breakthrough provides users an opportunity to enjoy up to an 8X performance improvement over VME64x without having to replace their existing VMEbus backplane via a "forklift" upgrade.

Texas Instruments announces new VMEbus driver

The technology to implement the 2eSST protocol on a standard backplane appeared when Texas Instruments announced the SN74VMEH22501 transceiver in April 2002. This transceiver is optimized for driving large capacitive loads with controlled edge rates and has tight input-switching thresholds of $1/2(V_{CC}) \pm 50mV$ for increased noise immunity. It utilizes a supply voltage (V_{CC}) of +3.3V and has +5V tolerant inputs to allow operation under the standard VMEbus legacy termination scheme. Full specifications, data sheets, device models, and sample requests are available through the TI Web site (www.ti.com).

VMEbus signal integrity testing

Motorola has worked closely with Texas Instruments for the past six months to test the SN74VMEH22501 transceiver in a variety of board configurations on standard 21-slot backplanes. Motorola's preliminary test results were first presented at the VSO meeting held on May 22, 2002, in Scottsdale, AZ. The test results are detailed in the sections that follow.

Test configurations

A test board that emulates several VMEbus protocols was designed to allow testing of the SN74VMEH22501 device in a realistic VME environment. The test board was a 6U VME board that could be configured as the master (driving board), slave (responding board), or receiver (non-participating board). For simplicity, the test board connected to a subset of VME signals, including the full data bus and selected control signals, to allow simulated VMEbus cycles.

Two 21-slot test chassis were used – one with a 5-row backplane, the other with a 3-row backplane. Typical chassis configurations consisted of one master, one slave, and multiple receiver boards. In order to observe a variety of loading conditions and identify worst-case configurations, approximately 55 different chassis population configurations were tested, some of which are shown in Figure 1.

Different transfer rates were tested, including 40 Mtransfers/sec (320 Mbytes/sec, 2eSST), 20 Mtransfers/sec (160 Mbytes/sec, 2eVME), and 10 Mtransfers/sec (80 Mbytes/sec, VME64), in both the 5-row and the 3-row chassis. Tests were also run comparing the performance of the SN74VMEH22501 to standard VMEbus drivers.

Effect of AC return caps

In the course of testing, Configuration 39 in Figure 1 was found to be worst-case with respect to non-monotonicity of the waveform measured on the slave board. In this configuration, data line D12 showed a large dip in the rising edge, actually re-crossing the threshold of the 2eSST device input. In the VMEbus pinout, D12 is in the middle of a group of eight data bits on P1/J1 Row C as shown in Figure 2. Signals on Rows A and B had significantly better signal integrity than those on Row C because they are closer to the many ground pins

Config Number	Chassis Slot Number																				
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
19	M	r	S	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
17	M	r	r	r	r	r	r	r	r	S	r	r	r	r	r	r	r	r	r	r	r
18	M	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	S
20	r	r	r	r	r	r	r	r	r	r	M	r	S	r	r	r	r	r	r	r	r
29	r	r	r	r	r	r	r	r	r	S	M	r	r	r	r	r	r	r	r	r	r
30	r	r	r	r	r	r	r	r	r	r	M	r	r	r	r	r	r	r	r	r	S
25	M										r						r	r	r	r	S
26	M										S						r	r	r	r	r
21	M									S											
27	M																				S
28										S	M										
39	M	S						r	r	r	r	r	r	r	r	r	r	r	r	r	r
78	M	S			r			r	r	r	r	r	r	r	r	r	r	r	r	r	r

M=master, S=slave, r=receiver

Figure 1. A sample of chassis population configurations

on Row Z in the 5-row VMEbus pinout. Testing indicated that two effects were causing the problem:

- The lack of an adequate AC return path in close proximity
- A chassis configuration that caused a large impedance discontinuity on the backplane

It was found that adding high-frequency capacitors to ground from the Row D power pins improved the Row C signal quality significantly. Figures 3 and 4, respectively, show waveforms measured on the slave board without and with the AC return capacitors. Although the voltage dip seen in Figure 4 came close to the positive input threshold of the SN74VMEH22501, its tight input thresholds of $1/2(V_{CC}) \pm 50\text{mV}$ did not allow the signal to propagate through the device and cause erroneous data. Empirical data showed that $0.022\mu\text{F}$ was the optimum value. It is recommended that the AC return capacitors be placed on each payload board on all of the Row D power pins flagged by arrows in Figure 2.

Effect of chassis population

Configuration 39 caused a large impedance discontinuity on the backplane because there was a large section of the backplane with no load (Slots 3-7) followed by a large fully loaded section (Slots 8-21). Time domain reflectometer (TDR) measurements showed the unloaded section to have an impedance of about 40 ohms, while the fully loaded section had an impedance of about 21 ohms. The reflection at this discontinuity caused the dip in signal D12 seen in Figure 3. If the chassis configuration was slightly modified to even out the impedance along the transmission line, the signal quality improved significantly. Figure 5 shows waveforms measured on the slave board for Configuration 78, which was identical to Configuration 39 except the receiver board from Slot 12 was moved to Slot 5. This evened out the impedance along the backplane, and the improvement in signal quality was evident. For this reason, it is recommended to distribute 2eSST boards evenly in the chassis for best noise margins.

Filters on VMEbus control signal

For years, filters have been used on VMEbus boards to mitigate crosstalk on certain control signals, most notably BBSY*. It was found that crosstalk on these signals with the new 2eSST driver was similar to the levels seen when using standard VMEbus buffers and that existing filter designs were adequate for

Pin	Z	A	B	C	D
1	MPR	D00	BBSY*	D08	VPC
2	GND	D01	BCLR*	D09	GND
3	MCLK	D02	ACFAIL*	D10	+V1
4	GND	D03	BG0IN*	D11	+V2
5	MSD	D04	BG0OUT*	D12	RsvU
6	GND	D05	BG1IN*	D13	-V1
7	MMD	D06	BG1OUT*	D14	-V2
8	GND	D07	BG2IN*	D15	RsvU
9	MCIL	GND	BG2OUT*	GND	GAP*
10	GND	SYSClk	BG3IN*	SYSFIL*	GA0*
11	RESP*	GND	BG3OUT*	BERR*	GA1*
12	GND	DS1*	BR0*	SYSRESET*	+3.3V
13	RsvBus1	DS0*	BR1*	LWORD*	GA2*
14	GND	WRITE*	BR2*	AM5	+3.3V
15	RsvBus2	GND	BR3*	A23	GA3*
16	GND	DTACK*	AM0	A22	+3.3V
17	RsvBus3	GND	AM1	A21	GA4*
18	GND	AS*	AM2	A20	+3.3V
19	RsvBus4	GND	AM3	A19	RsvBus11
20	GND	IACK*	GND	A18	+3.3V
21	RsvBus5	IACKIN*	SERCLK	A17	RsvBus12
22	GND	IACKOUT*	SERDAT	A16	+3.3V
23	RsvBus6	AM4	GND	A15	RsvBus13
24	GND	A07	IRQ7*	A14	+3.3V
25	RsvBus7	A06	IRQ6*	A13	RsvBus14
26	GND	A05	IRQ5*	A12	+3.3V
27	RsvBus8	A04	IRQ4*	A11	LI/1*
28	GND	A03	IRQ3*	A10	+3.3V
29	RsvBus9	A02	IRQ2*	A09	LI/0*
30	GND	A01	IRQ1*	A08	+3.3V
31	RsvBus10	-12V	+5V STDBY	+12V	GND
32	GND	+5V	+5V	+5V	VPC

Figure 2. 5-row VME P1 pinout

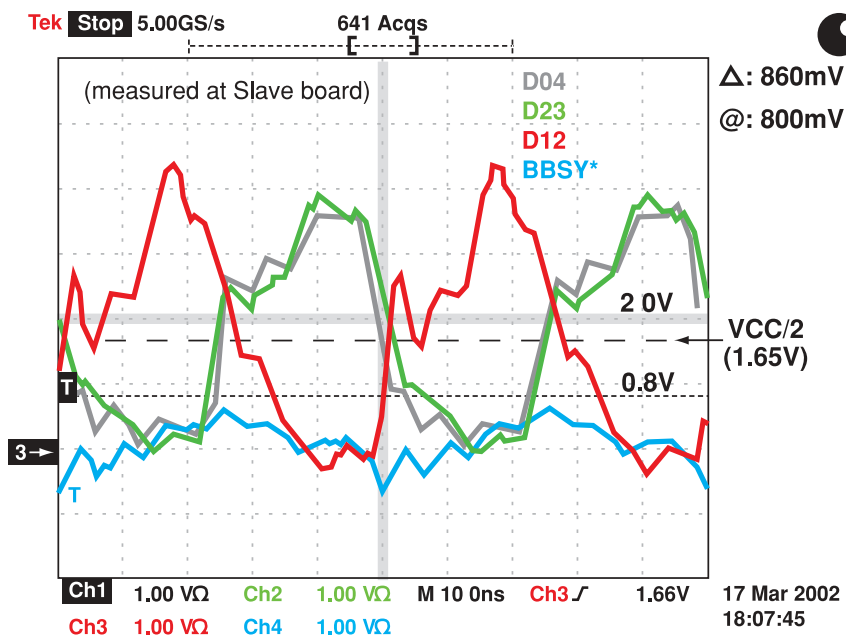


Figure 3. Configuration 39, no AC return caps

2eSST operation. For instance, a typical implementation for the BBSY* input would have a 100 ohm, 100 pF RC filter.

Other signal quality results

Testing indicated that reliable 2eSST operation was not likely on a 3-row backplane. At 2eSST speeds, the signal

quality was degraded unacceptably due to the relatively small number of ground pins in the 3-row VMEbus pinout. This confirmed the decision of the original VITA 1.5 (2eSST) working group to require the use of a 5-row backplane for 2eSST.



Testing also confirmed that a 3-row backplane was adequate for operation of the SN74VMEH22501 using standard VMEbus transfers (10 Mtransfers/sec or 80 Mbytes/sec). Performance was similar to that of standard VMEbus buffers.

Thermal testing

Thermal testing was also performed, comparing the operating temperature of the SN74VMEH22501 device to a standard SN74LVTH16245 buffer. Test conditions were as follows:

- 21-slot open chassis (no airflow)
- Driving board in Slot 1
- Load boards in Slots 2-21
- 2eSST data rates (40 Mtransfers/sec)
- 8 data buffers + 2 control buffers driven per device
- Thermocouple on the driving device

The steady-state temperature rises above ambient for both the SN74VMEH22501 and SN74LVTH16245 devices were 15°C to 17°C. This test confirmed that the typical power dissipation of the SN74VMEH22501 was similar to that of standard VME buffers.

Summary

Listed below is a summary of the conclusions drawn from the testing previously described:

- The SN74VMEH22501 device performs reliably for standard VME64 transfers on a 3-row backplane.
- A 5-row backplane is necessary for reliable VME 2eSST operation.
- System margins can be maximized by:
 - Adding AC return caps on 2eSST payload boards on Row D power pins
 - Distributing payload boards evenly in the chassis
 - Filtering VME control signal inputs
- The SN74VMEH22501 exhibits thermal characteristics similar to those of the SN74LVTH16245.



Bob Tufford has spent the last 17+ years designing computer system hardware and software. Bob joined the Motorola Computer Group in 1995 where he is currently a system architect, developing next-generation product architectures. His previous positions include system architect and lead engineer at Encore Computer Corporation and hardware engineer at Gould Computer Systems Division. Bob

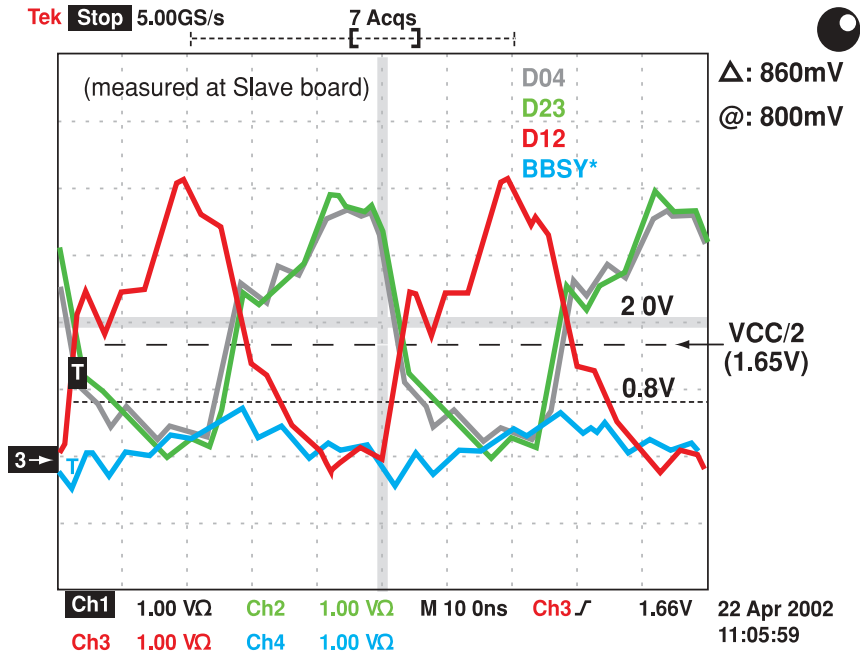


Figure 4. Configuration 39, 0.022uF AC return caps

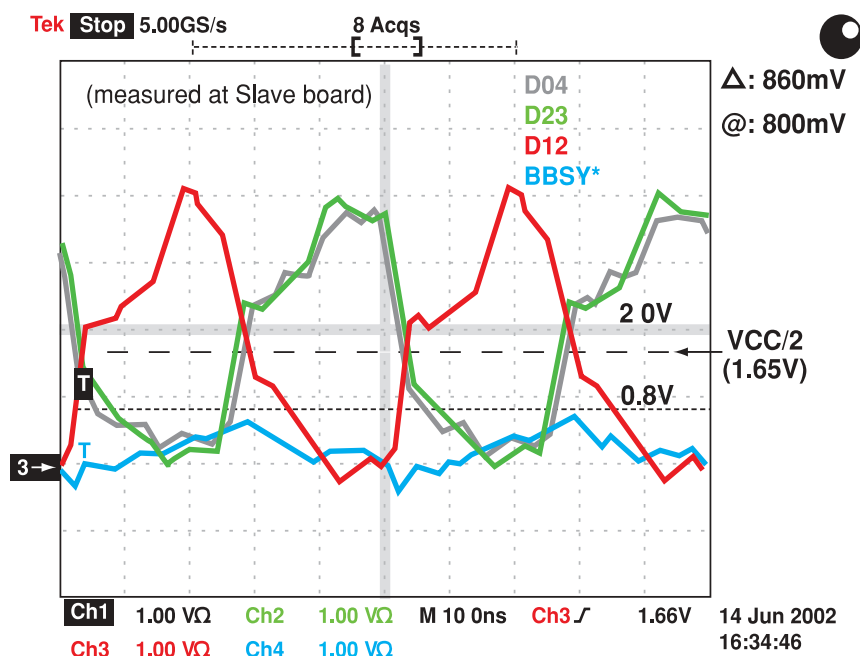


Figure 5. Configuration 78, 0.022uF AC return caps

holds a Bachelor of Science degree in electrical engineering and a Bachelor of Science degree in chemistry from Florida Atlantic University.



Mark German is a hardware design engineer with Motorola Computer Group. He has a BSEE from New Mexico State University and

has worked for 18 years in electronic hardware design at various divisions of Motorola.

For more information, contact:

Motorola Computer Group

Email: robert.tufford@motorola.com

mark.german@motorola.com

Web site: www.motorola.com/computer

