

Universal technology for the future

By Stefan Meissner

Boundary Scan is a very resourceful and advantageous testing technique. Manufacturers and developers sometime overlook the usefulness and capabilities of Boundary Scan, and therefore find they are missing out on the strategic advantages this technique can afford. From being impacting time to market to provide testing coverage of the entire life cycle of a product, Boundary Scan can prove to be a very valuable testing technique.

Boundary Scan

Boundary Scan, a resourceful test technique similar to the In-Circuit Test (ICT), but without physical contact, detects failure location, sets thousands of test points, and needs only four lines.

After lengthy discussions about the principle of testing through the stimulation and read-out of integrated thresholds in an IC during the 1980s, Boundary Scan (IEEE 1149.1) became a standard in 1991. Boundary Scan essentially means, *testing at the periphery (boundary) of an IC*. Besides the core logic and the contact points, some additional logic is implemented in an IC. These test points are integrated between the core logic and the physical pins. All Boundary Scan cells are combined in a shift register with parallel inputs and outputs and generate the serial scan path. In each Boundary Scan IC a control logic, the Test Access Port (TAP), is integrated to stimulate and read-out the cells. The IC is controlled by four signals. Asynchronous actions inside the TAP are executed at the edges of a Test Clock (TCK) signal where the TAP's single states are fixed at each increasing edge dependent on TMS (Test Mode Select). TDI (Test Data In) and TDO (Test Data Out) represent the input and output of the serial Boundary Scan shift register. Shown in Figure 1 is the typical structure of a Boundary Scan component.

A Boundary Scan test can be executed if all scan capable components are connected in a scan chain. The components must be manufactured with these Boundary Scan cells in order for the components to be effectively tested by Boundary Scan test tools. However, if at least one component on the board is Boundary Scan equipped, it is often possible to (partially) test other components on the boards, such as Flash devices. This can be in the case of

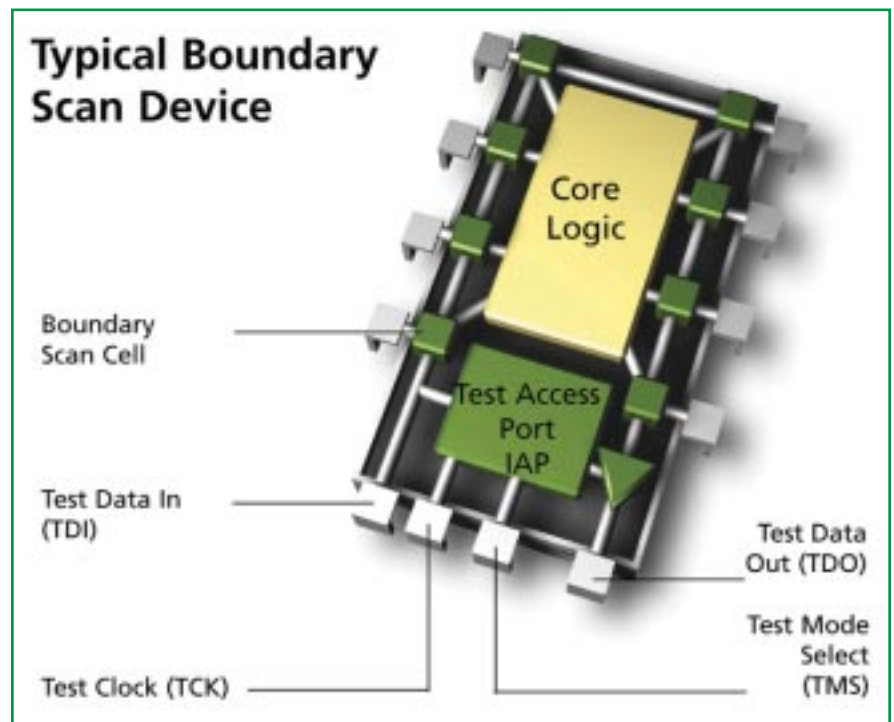


Figure 1

a Cluster test, where components that cannot be scanned are connected with Boundary Scan cells of some Boundary Scan ICs, and thereby these non-Boundary Scan components are capable of being tested.

There are various kinds of Boundary Scan tests:

- Infrastructure tests that check involvement of all scan capable ICs in the scan chain
- Interconnection tests that test all interconnected Boundary Scan nets
- RAM tests that test storage capabilities for each possible memory type. A RAM test is shown in Figure 2

- Cluster tests that test scan capable and non-scan capable components

How and where Boundary Scan is used

Boundary Scan is simple and universally adaptable. The technology supports a product throughout the entire life cycle. Already on the design stage, tests are possible by means of the CAD data, which can also be used later, all the way up to the customer's application. This means that a test pattern created for design verification can be reused for prototype debug and fabrication testing. This is an important advantage during the design of highly complex assemblies since testability for the future has to be considered. A depiction

BOUNDARY SCAN

SPECIAL FEATURE

tion of the use of Boundary Scan during the entire product life cycle is shown in Figure 3.

The time and effort required for testing is enormously reduced due to these facts. Only a few days or even hours are required to generate test programs, instead of the high efforts that accompany an In-Circuit test or functional test. Furthermore, diagnosis times are minimized, not to mention the high production costs of nail bed adapters (some tens of thousands of EURO). Tremendous capacities and long storage times for these adapters can also be avoided.

Likewise, by integrating Boundary Scan in ATE systems such as fixture-type systems or Flying Prober, test coverage can be increased further.

Boundary Scan's second field of application besides the assembly test is In-System Programming (ISP). The programming of PLD and FPGA ICs as well as the programming of Flash EEPROM ICs play an important role. PLDs and FPGAs are directly controlled by the Boundary Scan signals TCK, TMS, TDI and TDO. A program can be executed in compliance with the respective manufacturer conditions.

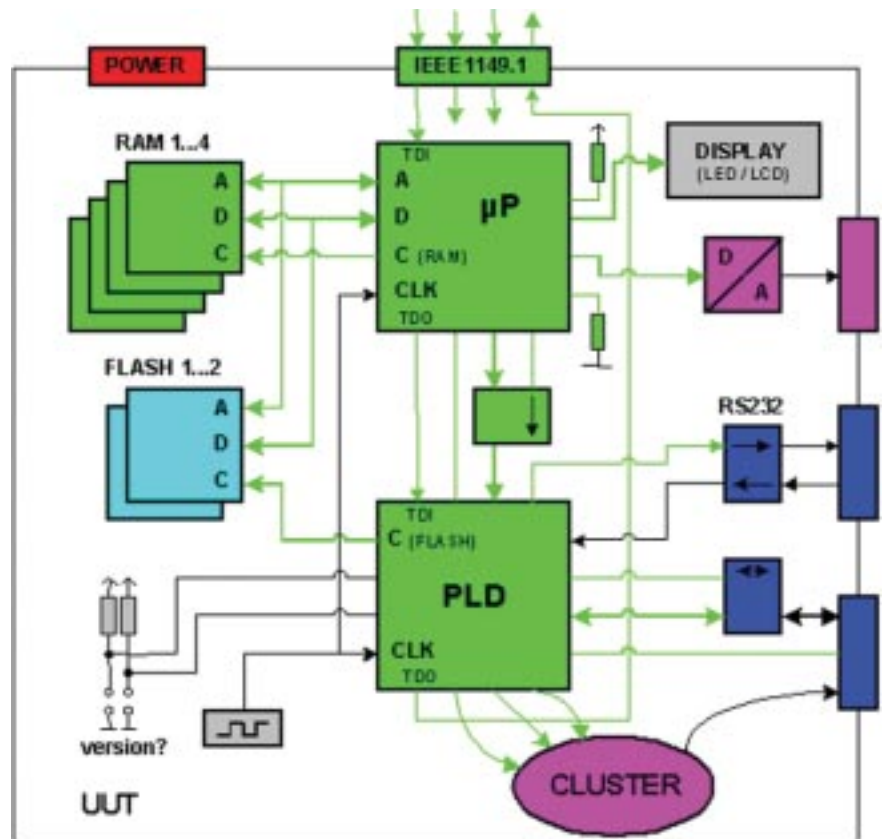


Figure 2

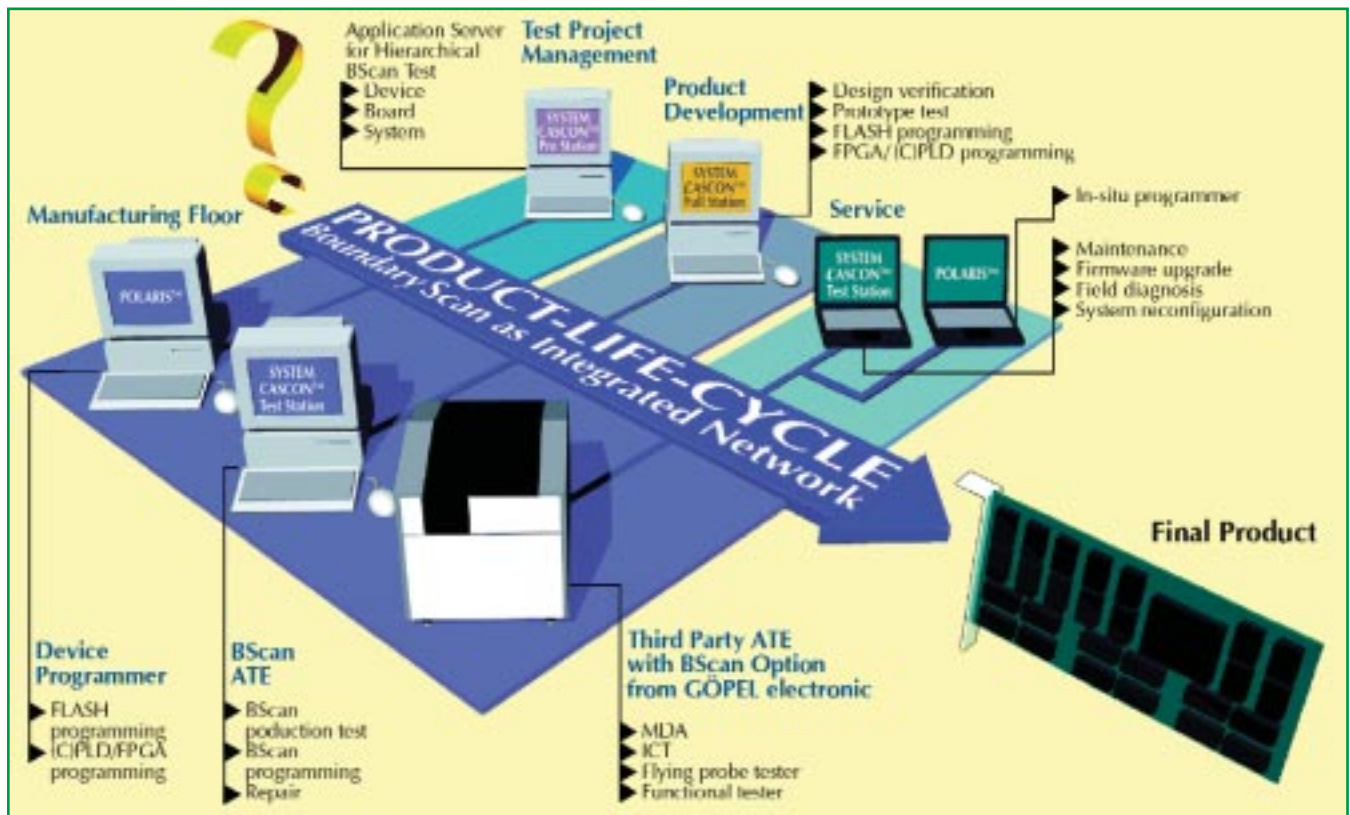


Figure 3

Flash programming is executed differently, since Boundary Scan pins control the signals of the flash ICs and the write and read accesses are recreated.

One of ISPs biggest advantages is the avoidance of separate steps in the assembly production because it can be tested and programmed in the same environment. Once they've been created, programs can be used again and again. Thus, the expenditure for reprogramming is minimal. This standardized process enables automated test set generation with accordant software support up to the pin level of diagnosis. By using a combination of various Boundary Scan tests, testability of a test object is increased even more.

Advantages of Boundary Scan

Using Boundary Scan accelerates the development of new products. The time that is saved in later stages of the PCB production shortens the total time-to-market and enormously increases market competitiveness since the ability to react much faster to trends and market requirements is enhanced.

This test technique also entails several cost reduction potentials. Alone, the investment required for the purchase of a Boundary Scan test system is far below the price of a functional tester or even an In-Circuit tester. Hundreds of thousands of dollars are no longer necessary to buy a complete test system. Due to the Boundary Scan testing concept the costs for development, production, and storage of nail bed adapters for the ICT don't apply. The test program creation via Boundary Scan is realized in a significantly shorter time. Last but not least, the diagnosis costs are reduced as a result of the high-test coverage (nearly 100 percent).

The continually increasing complexity and I/O connectivity of modern ICs such as PLD, Flash, or microprocessors in form of BGAs or μ BGAs nearly impedes a physical contact test. The only alternatives are visual inspection using X-ray or Boundary Scan. X-ray inspection has associated with it high investment costs and certain prejudices based on apparent health risks, making it the least desirable of the two alternatives. Due to the direct failure localization, high fault coverage rates are realized using Boundary Scan. Also, electric faults can be easily found using Boundary Scan, an advantage X-ray inspection doesn't have. Therefore, Boundary Scan technology completely lives up to the high demands on quality and stability of complex boards.



Figure 4

Outlook

Due to increasing access problems, static digital In-Circuit Test is going to be replaced more and more by the Boundary Scan technology. Remaining problems such as recognition of dynamic or analog failures can be covered by a combination of Boundary Scan with a Flying Prober or functional tester. There has been discussion about the standard's use for the analog test (IEEE 1149.4), but the number of ICs that support this process is relatively small and the current possibility for practical application is still in its infancy.

For digital testing in accordance with IEEE 1149.1, there is a high quality and mature system that has been used by manufacturers for years. One such example is SYSTEM CASCON (Figure 4) from GOEPEL electronic, and accompanying special hardware.

Hardware and software from low-cost solutions up to high performance systems are obtainable. Furthermore, there is a large amount of additional test tools, e.g. for the automated test set generation or the coupling with a Flying Prober or functional tester.

The advantages of Boundary Scan over conventional test technologies should always be considered. In the long run, the technology can't be ignored because who doesn't want to know the true promise of:

- Increased testability
- High fault coverage
- Shortened time-to-market
- Enormous cost reduction
- Sure product quality
- Increased competitiveness?



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