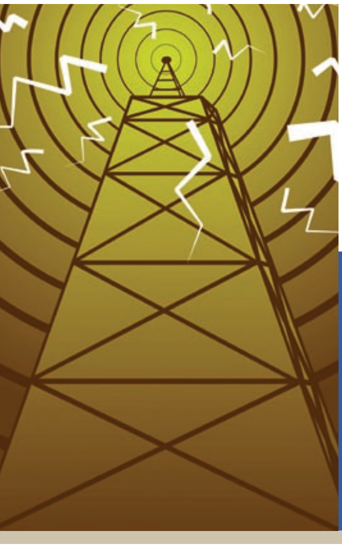


Smart component selection leads to high-functionality SDR designs

By *Robert Nokes*

The concept of hardware programmability, fundamental to the realization of Software-Defined Radio (SDR) systems, has over recent years stimulated the development of a variety of COTS-based hardware products that receive, process, and transmit radio signals. The design of present-generation data acquisition subsystems involves choosing hardware architectures and components that are crucial to their success. Trade-offs are inevitably made, and integrators must be aware of the effects those trade-offs have at the system level when they choose the individual building blocks. To reach the highest levels of functionality, paramount considerations include form factor, converter components, and onboard processing power – FPGA versus ASIC.

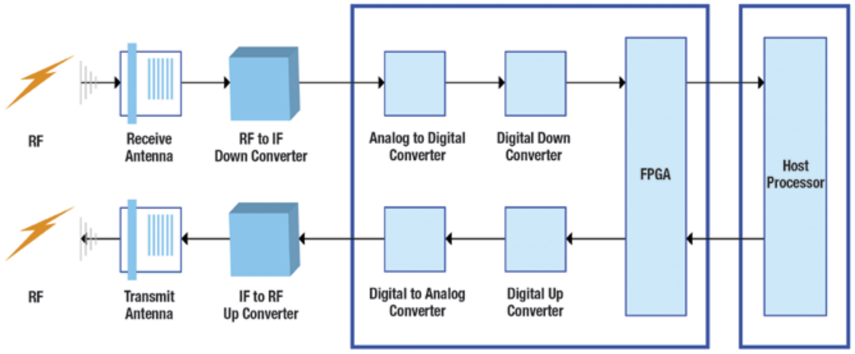
Software-Defined Radio (SDR) architectures can be used in a variety of applications using RF radio signals. For this reason, COTS modules such as digital receivers are not all created equal; thus, as new components become available, the standards by which they are judged become moving targets. COTS SDR module manufacturers make decisions on their architectures and performance trade-offs based on their perception of market needs. Integrators must be aware of the effects these trade-offs have at the system level, when choosing the individual building blocks. Considerations such as form factor, converter speed and resolution, and FPGAs versus ASICs should be at the core of the SDR development decision to ensure the highest functionality levels.

SDR: Building blocks of emerging technology

Software-Defined Radio is a rapidly evolving technology, devised to facilitate radio signal communication between platforms that could differ in terms of hardware implementation but which comply with guidelines published in a standard known as the *Software Communications Architecture* (SCA). Adopting this methodology ensures that radio communication parameters of compliant platforms are truly software-defined, meaning that they can be reconfigured at will via application software without the need to modify or replace any system hardware.

Several functional blocks are used in a typical SDR platform (see figure). Signals in the desired operating bands of the RF spectrum are routed via the receive/transmit antennae and then shifted by programmable analog down/up converters to an Intermediate Frequency (IF) that can be handled by the digital transmitter/receiver module, a key SDR building block that interfaces the IF analog receive and transmit signals to the digital processing domain via its Analog to Digital Converter (ADC) and Digital to Analog Converter (DAC) devices respectively. The ADC digitized output is known as a *wideband signal* since it contains the entire frequency spectrum sampled by the ADC.

Narrowband signals lying within this wideband signal can be tuned, extracted, and converted to baseband signals by the Digital Down Converter (DDC), while the Digital Up Converter (DUC) applies the inverse function in the transmit path. The FPGA provides the programmable resources needed to implement SDR signal processing functions known as *waveforms*, which can be downloaded as firmware. Finally, the host processor transfers FPGA data and control information via a bidirectional interface and runs the SDR application.



Form factor

The form factor of the SDR building blocks can be a critical decision factor. A COTS module's performance characteristics may be compelling, but if it does not meet the system's space, weight, and power limits, it is a nonstarter. For example, the larger Eurocard form factors (6U VME, CompactPCI, and especially AdvancedTCA) offer significant DSP resources and power dissipation capabilities, and their pin and socket style connectors provide reliable interfaces, even under high shock and vibration. But they are simply too large for any man pack or handheld application.

In addition, some form factors are simply not tolerant of harsh environments (particularly vibration). PCI slot cards used in server class PCs are an example of a form factor offering impressive electrical and DSP performance at an attractive price point; however, the edge style connector does not tolerate vibration well, and adapting this kind of platform to challenging vibration environments (fixed and rotary wing aircraft, and even submarines) is often impractical, if not impossible.

PMC modules offer a highly portable form factor, one that has been embraced by VME and CompactPCI SBC and DSP manufacturers. The specification provides both conduction- and convection-cooling options, and the size is attractive in systems where portability is a key requirement such as man packs and UAVs. However, PMC modules impose challenging power and real estate limits on designers: PMC modules often feature fewer channels and less onboard processing power than larger form factors.

Converter components: Speed/resolution trade-off

ADC and DAC components often make or break an SDR system. In general, as speed goes up, resolution goes down. Higher conversion rates allow more bandwidth to be digitized, but higher-resolution samples provide more dynamic range (the difference in amplitude between the strongest and weakest signals that can be simultaneously digitized).

While a communications system designer may want to carry as much bandwidth as possible, high usage of the spectrum of interest is likely to include strong interfering signals as well as weaker signals of interest. The dynamic range requirement imposed by the different signal amplitudes will likely define the number of bits required. For example, suppose a small signal needs to be recovered in the presence of a much larger signal and all signals of interest lie in a 40 MHz bandwidth. The dynamic range required to do this is the difference in signal amplitudes (60 dB) plus an adequate operating margin to demodulate the signal, perhaps 10 dB. Sampling theory dictates that the sampling frequency must be at least twice the signal bandwidth. These requirements can be satisfied by a good quality 14-bit ADC which, when sampled at 100 MHz, would provide a dynamic range of at least 80 dB (see Figure 1).

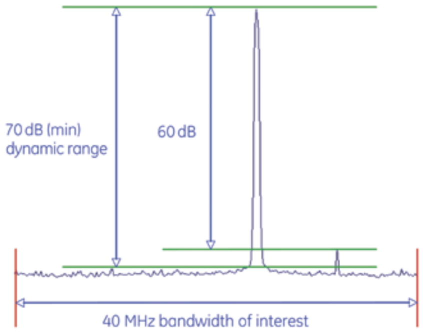


Figure 1

Onboard processing power: ASIC or FPGA?

A key trend in SDR has been the movement of the digital domain toward the antennae as ADC/DAC components increase in speed and resolution. But this imposes the problem of moving huge amounts of data to or from back-end DSP engines. When even the highest throughput buses fail to move the data fast enough, designers move their DSP engines. As a result, processing engines are following right behind the ADCs, toward the antennae.

The objective is to eliminate redundant data from further processing or movement as soon as possible. This introduces new complexity to selecting a COTS module: Which kind of DSP is required, and how much? While ASIC solutions offer power- and cost-efficient implementation of commonly used processes (DDCs are a very common example), they lack the flexibility of FPGAs.

While an ASIC-based, DDC-intensive design may excel at narrowband communications, it may be totally unsuitable for wideband applications such as radar or even some spectrum monitoring applications. Furthermore, the ability of an ASIC-based design to adapt to new waveforms can be limited by the functionality the ASIC designers had the foresight to include, while an FPGA-based product can see large benefits from information only available in hindsight.

Practical receiver architecture

The quad-channel digital receiver shown in Figure 2, the ICS-554 from GE Fanuc Intelligent Platforms, is an example of an SDR COTS product with a feature set aimed at radio communications and a wide range of other software-defined applications, such as Signals Intelligence (SIGINT) and small radar systems.

The quad receiver can handle up to four antenna signals simultaneously, each signal being individually sampled (typically at 100 MHz) by an ADC with a resolution of at least 14 bits in order to achieve an adequate signal/noise ratio in radio applications. Simultaneous signal sampling allows the phase difference between multiple antenna signals to be precisely calculated, a feature used in civilian and military applications to create antenna arrays with directional sensitivity that can be software-controlled.

Each ADC output is fed to a bank of four quad DDC devices (Texas Instruments GC4016), which can extract up to 16 narrowband signals from any of the four ADC wideband signals and is connected directly to the FPGA. The selection of ADC or DDC output data is determined by FPGA firmware under external host processor control, an important feature that offers users the trade-off of performing digital down conversion either in dedicated DDCs (superior performance but higher cost) or as FPGA firmware (more flexible but higher power consumption).

FPGA output is buffered in two large FIFO memories for eventual DMA to an external host processor via the PCI bus interface. FIFO memory – which allows data to be written into and read from its array at independent data rates – provides a high-density but low-power means of buffering output data since many applications process data in a single pass. Incoming data can thus be processed by the user

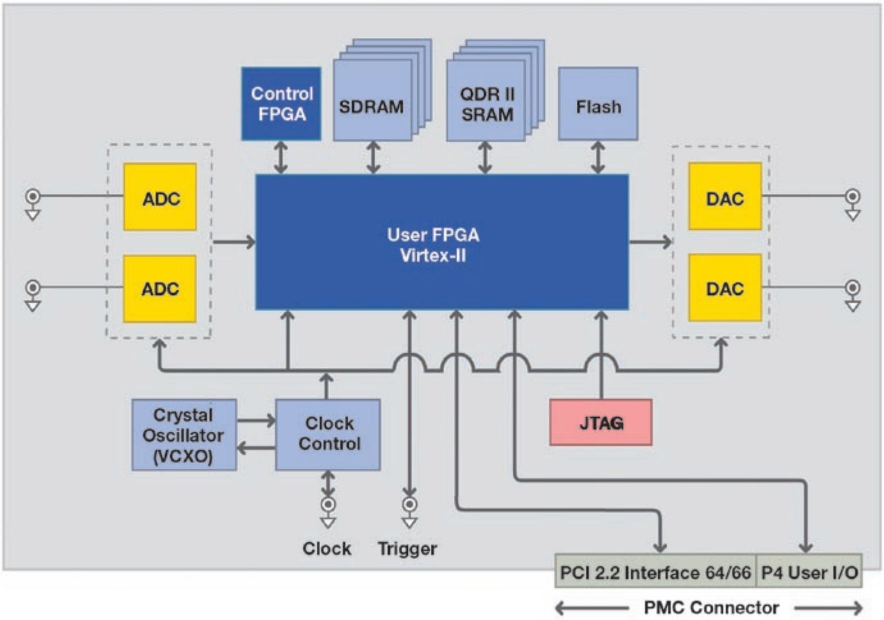


Figure 2

FPGA and then dumped into a FIFO, rather than being cycled in and out of SRAM. FIFO storage is also particularly suitable for accumulating data captured in bursts, such as pulsed radar returns. The dual output FIFO arrangement allows signals of differing bandwidth to be streamed simultaneously – an operating mode extensively used in SIGINT applications when narrowband signals need to be examined without interrupting the recording or analysis of a wideband scan.

Achieving SDR design goals

The design goal of any SDR board is to maximize performance within the physical and environmental constraints imposed by the intended application. Additionally, well-balanced overall system design together with astute component selection via form factor, converter speed/resolution, and ASIC versus FPGA performance will ensure that any functionality compromises are minimized. **CS**

Robert Nokes *is a field applications engineer for GE Fanuc Intelligent Platforms, specializing in high-performance data acquisition products for commercial and military embedded system designs. Having obtained a bachelor's degree in Engineering Science at Oxford University, he has worked in the consumer, semiconductor, and military electronics industries at a number of companies including ITT and Texas Instruments. He joined GE Fanuc Intelligent Platforms (formerly Radstone) in 2002.*

GE Fanuc Intelligent Platforms
703-263-1483
www.gefanuc.com

SDR 101: Basic decisions

While there are many design factors that should be considered up-front when developing a new SDR application, functionality and cooling are basic yet important variables in the equation.

Functionality: RX, TX, XX

A wide range of applications, including radio, telecom, SIGINT, and radar can all use SDR techniques and hardware to advantage. Some involve only reception, some only transmission, and some both. While combining multiple modules can yield higher functionality (for example, separate RX and TX modules could be combined to provide transceiver capability), an additional clock generator module may also be required to achieve precise synchronization of TX and RX signals. Using a transceiver module with onboard synchronized RX/TX clocks that can be frequency-locked to an external master clock could be a more manageable approach under these circumstances.

Cooling: Convection or conduction?

Because the military is a primary SDR technology user, harsh environments often characterize deployment. Until recently, few COTS vendors offered truly rugged SDR products, and many still do not. The majority of SDR products currently offered are simply not suitable for zero airflow situations. Conduction cooling is a key differentiator among COTS SDR product vendors.