

VITA 56 – A fabric-based PMC replacement mezzanine specification

By David Slaton

In 2005, a VSO VITA 56 working group was established to specify a new mezzanine card that could replace the aging PCI Mezzanine Card (PMC) in 6U embedded systems. This mezzanine card, also known as Express Mezzanine Card (EMC), will offer embedded systems an expansion option that supports the latest and future multi-Gigabit serial fabrics and provides greater levels of manageability and serviceability. These include the ability to remove the module from its host through the front panel. In the first half of 2007, the base EMC specification (EMC.0) will be released under VSO guidelines for trial use.

Parallel bus on the decline

Prior to the advent of serial fabrics such as PCI Express and Serial RapidIO in embedded systems, the parallel PCI bus was predominately used to interface single board computer chipsets to various I/O controllers. Although the PCI bus scaled over time to accommodate greater I/O bandwidth demands, the limitations of parallel bus technology began to become a bottleneck. During that time, the PMC was adapted to support higher-speed parallel I/O through the VITA 39 effort, which added PCI-X capabilities to the module.

To further extend the PMC's life, XMC (VITA 42) was created to provide serial fabric capabilities. This was accomplished by adding two additional connectors to the module, one for the serial fabric and another for optional fabric or I/O. However, because of the overriding goal of backwards compatibility, XMC does not address issues such as front panel module insertion/extraction – which improves system serviceability – and poor placement of mounting holes, keying pins, and board-to-board connectors on the PMC, which hinders high-speed I/O support. Furthermore, there exists today a question about the ability of the chosen connectors to scale in speed to support emerging fabrics, potentially limiting top-end mezzanine performance.

The VITA 56 working group set out to start anew with a module specification that would retain the PMC's physical volume, allowing two modules per 6U carrier but providing support for the latest serial fabrics. Realizing that an existing module specification (Advanced Mezzanine Card or AdvancedMC)

offered many of the features sought for a 6U mezzanine, the VITA 56 working group started with AdvancedMC. The working group then made substantial but necessary changes to create a module more suitable to traditional and future embedded systems. Table 1 contains various subspecifications that make up the VITA 56 specification.

a “fat pipes” region, and a “common I/O options” region.

Because the EMC is seen as a replacement for PMC, where a parallel PCI bus was the main I/O channel, the working group identified PCIe as the first fabric to be supported. As part of the base specification, a set of ports on the connector

VITA Name	Industry Name	Description
VITA 56.0	EMC.0	Base Specification, Convective-cooled Version
VITA 56.10	EMC.10	Base Specification, Conduction-cooled Version
VITA 56.1	EMC.1	PCIe Signal Protocol on VITA 56
VITA 56.2	EMC.2	GbE on VITA 56
VITA 56.3	EMC.3	Storage on VITA 56
VITA 56.4	EMC.4	Serial RapidIO on VITA 56
VITA 56.20	EMC.20	Common Option I/O Routing
VITA 56.99	EMC.99	Vendor Part Number List

Table 1

Where we are with VITA 56

The VITA 56 working group's first priority has been to detail the fabric requirements for PCI Express (PCIe), the mechanical requirements for the module and carrier, the module/carrier management mechanism, and general I/O configurations. The subspecifications that relate to these areas are EMC.0, EMC.1, and EMC.20. The base specification EMC.0 details the mechanical requirements and other general requirements for a module and carrier. The base specification also defines the port mapping strategy for EMCs, as shown in Table 2.

The base specification defines “ports” or differential transmit/receive pairs for several uses: clocks, a base PCIe channel,

is allocated for a PCIe channel (up to a x4) that is present on all modules. A subspecification for PCIe, EMC.1, has been created to detail PCIe use on the ports in the “fat pipes” region.

Mechanically, the EMC maintains the 10 mm board-to-board spacing first used by the PMC and generally has the same dimensions and volume (see Figure 1) but uses a card-edge connector system that allows the module to be removed



Figure 1

through the front panel. Just like on a PMC, the main component side of the module (facing the carrier) has a maximum component height of 4.7 mm as does the maximum component height of the carrier underneath the module, except near the front panel, where the module is allowed to occupy the full volume.

To facilitate module removal, a thumbscrew is included on the module's front panel and engages a switch on the carrier to indicate the insertion/removal status (Figure 2) so important in the management of hot-swappable resources. The thumbscrew also serves as a positive retention mechanism by locking into a retention block on the carrier.

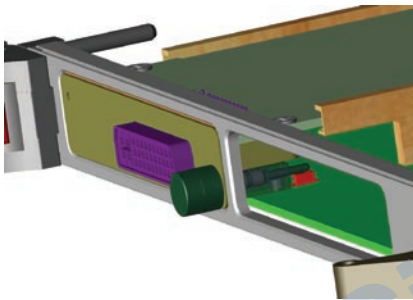


Figure 2

The working group has also dealt with the issue of module management, balancing the need for low-cost module development while providing for the increasing need of systems to monitor and control a variety of module parameters. The VITA 56 specification defines Unmanaged Modules (UMs) where on-module management resources are not required and Managed Modules (MMs) where the module contains a management controller that interacts with a controller on the carrier or elsewhere in the system.

To ensure the compatibility of a UM with the carrier, the specification defines a table of acceptable "fat pipe" configurations. These configurations are designated by the carrier through the use of four signals, PS0D#-PS0A# (Table 3). For example, a UM may support two independent x8 PCIe links (referred to as "EMC.1b" in the table), as shown in Figure 3.

If the module and carrier agree that the designated configuration is supported, a handshaking signal is activated and the carrier may enable the module.

MMs negotiate fabric compatibility through an I2C bus using Intelligent Platform Management Interface (IPMI)

Part No.	EMC Port Mapping Strategy	
CLK1	Clocks	
CLK2		
CLK3		
0	X1	Base PCIe
1	X2	
2		
3	X4	
4	Fat Pipes Ports 1-12	
5		
6		
7		
8		
9		
10		
11		
12		
13		
14		
15		
16	Common Options	
17		
18		
19		
20	Undefined	

Table 2

PSx# Decoding				
PS0D#	PS0C#	PS0B#	PS0A#	Meaning
0	0	0	0	Bus Negotiated via IPMI
0	0	0	1	EMC.1a – PCI Express "a"
0	0	1	0	EMC.1b – PCI Express "b"
0	0	1	1	EMC.1c – PCI Express "c"
0	1	0	0	EMC.2a – GbE "a"
0	1	0	1	EMC.2b – GbE "b"
0	1	1	0	EMC.2c – GbE "c"

Table 3

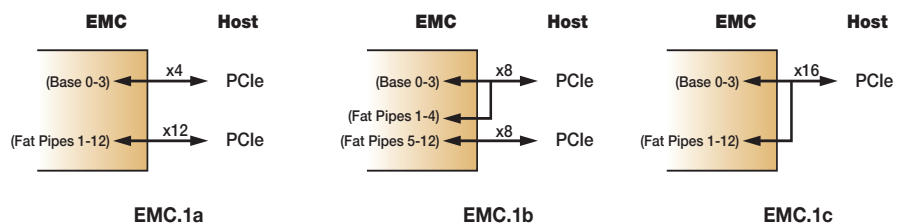


Figure 3

request/responses and e-keying methods similar to those used in AdvancedMC management. The VITA 56 specification defines a subset of IPMI commands required to properly enable the module while minimizing the management resources needed on a module.

“As the use of the PMC fades because of lack of support for parallel PCI buses in chipsets and peripheral components, modules like EMC will begin to proliferate.”

In addition to fabric negotiation, the VITA 56 specification defines several I/O configurations that are supported to allow compatible egress of “common” signals such as Ethernet, Serial ATA, USB, and so forth, via the EMC.20 subspecification. On MMs, these configurations are instead negotiated through carrier/module I2C transactions, similar to how the “fat pipes” ports are configured. The EMC.20 subspecification also details pertinent routing between modules and backplane connectors on various carriers including VITA 31.1, 41, 46, and PICMG 2.16.

EMC usage

The EMC is a module suitable for general purpose I/O expansion based on serial fabrics like PCIe and Serial RapidIO. As the use of the PMC fades because of lack of support for parallel PCI buses in chipsets and peripheral components, modules like EMC will begin to proliferate. This is especially important given that the 6U form factor has a long life ahead of it as VME and CompactPCI platforms continue to be created, and as new 6U standards like VITA 41 and 46 become more mainstream.

As new platforms emerge supporting serial fabrics, more opportunities exist for EMCs to be used in ways similar to how AdvancedMC is used in AdvancedTCA

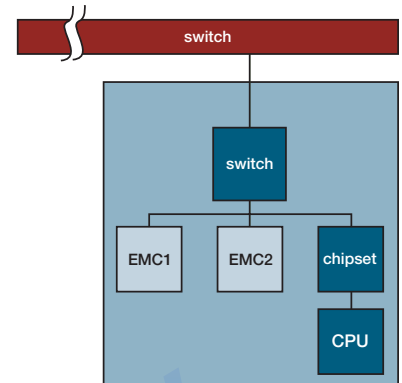
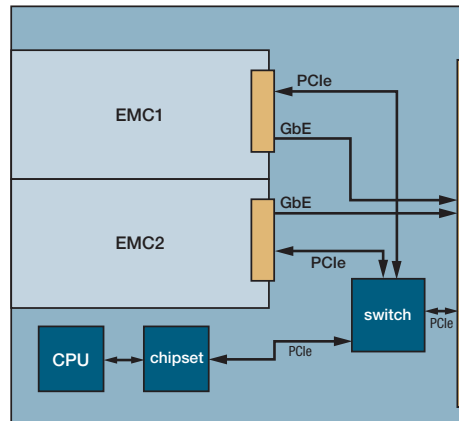


Figure 4

and MicroTCA systems (left side of Figure 4). In such systems, the carrier is an extension of the larger “system” as a node on a hierarchy (right side of Figure 4), with the modules as simply another extension. Such fabric-based systems provide multiple parallel data paths for local data traffic and greater throughput over traditional parallel systems.

New mezzanine standard

Regardless of the topology used in a given fabric-based system, any new module or carrier must be scalable to provide a service life comparable to systems making use of parallel buses such as VME or CompactPCI. Today, fabric standards support data rates of a few Gbps, but emerging standards support 10 Gbps or more. Unlike current mezzanine solutions that provide connectors capable of transmission in the 3-10 Gbps range, the connector chosen for EMC is specified for up to 12.5 Gbps, and variants have been demonstrated to perform under strict routing conditions in excess of 20 Gbps.

Modern systems are also increasingly required to provide higher levels of serviceability such that systems can remain operational while faulty subsystems are replaced. The ability to remove the module without removing the carrier and support for hot swapping make the EMC ideal for such highly reliable and serviceable applications as telecom central offices.

VITA 56 defines a mezzanine that is flexible enough to support a variety of

fabrics and scalable to accommodate higher speed signaling. It also provides management for greater system reliability and hot swapping for increased serviceability. As a result, the EMC is poised to be the ubiquitous mezzanine solution for future embedded systems. **CS**



David Slaton is a senior NPI design engineer for GE Fanuc Embedded Systems and has worked on embedded systems design for

14 years. During the past nine years, he has worked on VME, CompactPCI, AdvancedTCA, and AdvancedMC designs ranging from high-speed data I/O boards to Intel-based single board computers. He holds a BSE from the University of Alabama in Huntsville.

To learn more, contact David at:

GE Fanuc Embedded Systems
 12090 S. Memorial Pkwy.
 Huntsville, AL 35803
 256-880-0444, Ext. 222
 david.slaton@gefanuc.com
 www.gefanuc.com/embedded