

Power Architecture's evolution provides DSP advantages

An ongoing series magnifying Power Architecture technology trends enhancing Aerospace & Defense (A&D) solutions



UNDER the μ SCOPE

By Katie Butler and Ian Stalker

Today's defense and aerospace system designers have a wide variety of choices when it comes to selecting their next DSP system architecture. The DSP and general processor market space is crowded with discrete DSP architectures and processor architectures including MIPs, x86, ARM, and Power Architecture-based product offerings that cover a wide range of performance, power, and price objectives. Yet among the vast array of choices, Power Architecture remains one of the few dominant architectures that continually meets the specific needs of military and aerospace systems. Why has this architecture, which was introduced in the early 1990s, continued to dominate this particular market space? Will it continue to lead in the future? The answers lie in the historic evolution of the architecture, which has resulted in low-power, high-performance products targeted at embedded applications. The architecture continues its evolution into highly integrated solutions that help solve future complex applications.

Power Architecture's evolution

The original PowerPC architecture developed by Apple, IBM, and Motorola came from IBM's Performance Optimization with Enhanced RISC (Power) architecture. Although the original PowerPC architecture was focused on desktop systems, it evolved into several Instruction Set Architectures (ISAs) optimized for various applications. Book E, one of the ISAs (Figure 1), was developed with a focus on the embedded market, and it included only a single book that had both user- and supervisor-level components in one place. This ISA created a processor solution for many of the A&D systems where both performance and power dissipation in an embedded application were crucial. Since that time, the

PowerPC architecture has evolved into the Power Architecture, with innovations in vector processing and power management that have provided embedded designers with a long history of balance between performance and dissipation.

One of the improvements made to the Power Architecture was the AltiVec Single Instruction/Multiple Data (SIMD) instruction set. This extension was introduced in 1999 as part of the MPC74xx processor that powered Apple's G4 Macintosh computers. This innovation also provided the DSP world a breakthrough alternative to dedicated DSP chips, as AltiVec technology did the required vector processing within the core processor. Many military applications require the support for floating point math that the AltiVec technology provides, as floating point calculations are much more efficient than fixed point math but typically require additional silicon. Unlike commodity electronics applications, which are much more cost

sensitive, military and aerospace systems put a higher premium on efficiency and demand floating point support. It is interesting to note that the AltiVec instruction set was never formally part of the PowerPC architecture until Power.Org officially united it in their ISA 2.03 release.

AltiVec technology is the standard approach today for many aerospace and defense DSP applications, and it supports a wide variety of readily available RTOSs. Without support for standard RTOSs, dedicated DSPs presented a much more difficult programming paradigm than the Power Architecture technology, which offered access to superior tool chains supported by numerous third-party vendors.

Another key Power Architecture advantage is the focus on lower power dissipation through integration. As the demand increases to deploy more processors in the space-constrained environments

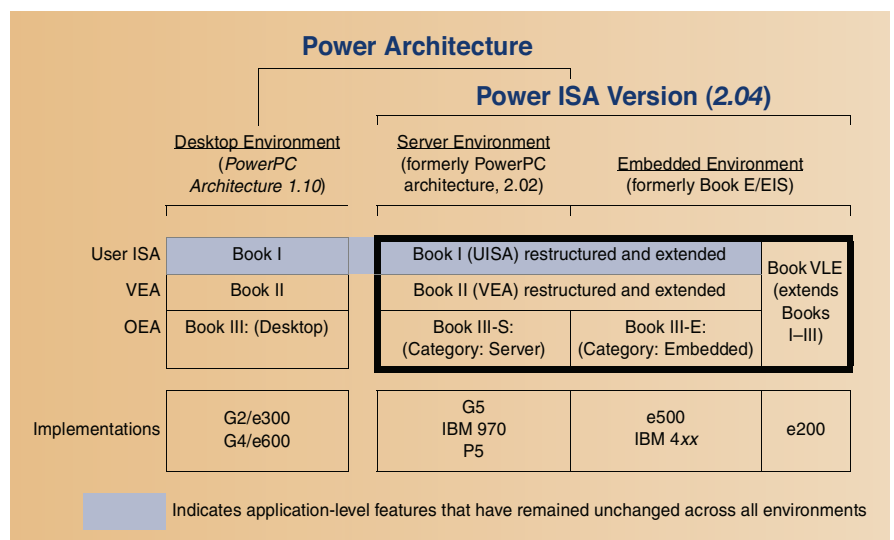


Figure 1

common to VME and VPX systems, Power Architecture technology vendors have begun integrating more processor cores within a single die. One specific example of this is the dual core MPC8641D from Freescale, as it delivers twice the performance with a significantly reduced power burden as compared to the single core version of the processor. With more features integrated into the die, reliability and performance have increased while the chip count has been reduced. This saves valuable board space, which is a critical issue for military and aerospace designers. Moreover, the higher levels of integration save system power because individual chips use more power for the same functions residing on a single device.

Today's innovations for A&D applications

Power Architecture technology is continuing to evolve with a focus on integration as the proliferation of radar and signal processing applications is making SWaP (Space, Weight, and Power) increasingly critical. One key improvement that can be found in some Power Architecture technologies is the inclusion of multiple memory controllers. These built-in memory controllers improve system speed by lowering latency and supporting higher bandwidths on the memory bus. This is a great benefit for DSP systems, which are high consumers of DRAM bandwidth, as they frequently read out of DRAM to handle large amounts of incoming data. Without the ability to adequately handle the data, a high-performance internal core can become stalled while waiting for incoming data from memory. One example of this usage is the Curtiss-Wright CHAMP-AV4 VME DSP engine, which uses the earlier Power Architecture technology MPC7448. It uses a separate Marvell Discovery III memory bridge, delivers 125 MHz DDR memory interface with a peak performance of 2 GBps. Today, the MPC8641-based CHAMP-AV6 VPX DSP engine (Figure 2) uses DDR2 memory at twice the speed with two memory banks instead of one, to deliver a 4x improvement in memory speed.



Figure 2

As application requirements have evolved, image processing systems have driven the demand for large, scalable multi-processor systems. A key advantage for Power Architecture technology versus x86 architected processors is its built-in support for Serial RapidIO fabric technology. Unlike GbE and PCIe fabrics, the Serial RapidIO fabric provides integrators the ability to build arbitrary topology-based networks. Serial RapidIO fabric is a true peer-to-peer multiprocessing network technology, using an endpoint and switch model. The endpoint is the chip itself, which communicates to other endpoints through one or more interconnected Serial RapidIO switches that collectively constitute the Serial RapidIO “network” or “fabric.”

Unlike other fabrics, Serial RapidIO has no rules that force the use of specific topologies, which makes it very flexible and enables very large systems to be built with up to 65,536 nodes – far beyond the needs of a typical COTS system. In multiple processor applications, the ideal scenario is numerous processors that can all connect with each other at high speeds on an equal basis, without any of the processors having special attributes, unlike PCI/PCI Express systems where one processor is the root. The Serial RapidIO feature of the MPC8641D, with supporting Serial RapidIO switch chips, is the key technology that allows board designers to harness the bandwidth capabilities of the new VPX (VITA 46) standard.

Looking toward the future of Power Architecture

Power Architecture, with its embedded market background, has had a long history in the A&D market. Power Architecture technology’s future lies largely in the hands of the Power.Org organization, which was chartered in 2004 with the responsibility to develop open standards and specifications for the architecture. The merged Power ISA 2.03 has been announced and provides a pathway forward for Power Architecture vendors and end users.

Although there are many choices for system designers, the Power Architecture offers many key advantages that help to simplify board design, reduce power, and provide high bandwidth connectivity for complex DSP applications. Historically, Power Architecture technology has provided low-power, high-performance processors used widely in defense and aerospace systems; its evolution has led to highly integrated solutions that combine vector processing, multiple memory

controllers, and serial switched fabrics such as Serial RapidIO. This evolution continues to help designers reduce space, weight, and power, all of which are critical in defense and aerospace systems. It also appears that Power Architecture technology will continue to be a dominant architecture in future defense and aerospace DSP designs. **CS**



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