VITA Standards Update

By John Rynearson

E-cast

VITA 42.0 receives ANSI recognition, VITA 46.14 tackles analog and RF on VPX

Editor's note: *The following update pertains to the January 2009 VSO meeting.*

Be sure to check out our online E-cast archives for the latest video and audio updates on VITA 41, 46, and 48. See www.opensystemsmedia.com/ecast.

VSO ANSI accreditation

Accredited as a Standards Development Organization (SDO) in June 1993 by the American National Standards Institute (ANSI), the VITA Standards Organization (VSO) meets every two months to address vital embedded bus and board industry standards issues. Information on ANSI/VITA standards is available on the VITA website at www.vita.com.

VSO study and working group activities

Standards within the VSO may be initiated by a study group and developed by a working group. A study group requires the sponsorship of only one VSO member and is used to build interest in a standard. A working group requires the sponsorship of at least three VITA members, and the proposed work must fit within the defined scope of VITA's accreditation with ANSI.

VITA 17.2, Serial Front Panel Data Port (SFPDP) Channel Bonded Protocol

Objective: Increase the bandwidth for FPDP to include data rates of 2.5, 3.125, 4.25, and 6.25 and provide channel bonding for 2x, 4x, 6x, 8x, and 12x lanes.

Status: Janusz Kossek, Curtiss-Wright Controls Embedded Computing (CWCEC), will assume the chair position to replace Ralph Barrera. There are only a few outstanding issues that need to be addressed before the draft is submitted to ANSI ballot.

VITA 41.6, VXS 1x GbE Control Channel Layer

Objective: To define and assign 1x GbE signals for communication over signal sets currently defined as reserved for future use in VXS.0.

Status: VITA 41.6 has completed its ANSI recirculation ballot. One negative ballot has turned into a positive vote. VITA 41.6 will be submitted to ANSI for recognition after Feb. 2, the cutoff date for negative ballot notification.

VITA 42.0, XMC

Objective: Expand PMC to include serial fabrics.

Status: VITA 42.0 has been recognized as an ANSI standard. VITA 42.6 has completed a working group ballot. Wai Ho Wu, the draft editor, will update the draft. VITA 42.20 will add support for 1 GbE to XMC as a separate control plane. The goal is to support P15 alone.

ANSI/VITA 46.0, VPX

Objective: Define a standard for VME based on 1101.2 with new connector.

Status: Jing Kwok, CWCEC, provided an overview of VITA 46 activities and reviewed the agenda for the recent full-day working meeting.

VITA 46.14, RF Interconnect on VPX

Objective: Develop a standard for analog and RF interconnects on VPX via the backplane.

Status: The goal of VITA 46.14 is to provide a method for interfacing to analog and RF signals on VPX modules through a backplane interface. Jim Reedy, DRS-SS, discussed comments received on the current draft and reviewed the results of recent electrical tests.

VITA 47r2, Environmental Requirements

Objective: Add EMC requirements to ANSI/VITA 47.

Status: VITA 47r2 is a revision of ANSI/VITA 47 to add ESD requirements per IEEE PAR-1688 and to add an additional environmental class. 47r2 will be completed once 1688, which is out for review, is stabilized.

VITA 48.0, Mechanical Specifications for Microcomputers Using Ruggedized Enhanced Design Implementation (REDI)

Objective: To define a mechanical design for two types of plug-in units: Type 1 supports 2 Level Maintenance while Type 2 does not.

Status: Mike Gust, Mercury Computer Systems, reviewed VITA 48 activities and discussed outstanding issues to be reviewed at the working group meeting.

VITA 49.0, VITA Radio Transport (VRT)

Objective: To define a transport-layer protocol designed to promote interoperability between RF receivers and signal processing equipment in a wide range of applications.

Status: VITA 49.0 and 49.1 have successfully completed ANSI ballot. Public review ends Feb. 2. Comments will be reviewed and results will be submitted to ANSI for recognition.

VITA 51.2, Physics of Reliability Failure

Objective: This effort will look at the physics of failure as it relates to ANSI/VITA 51.0 and 51.1.

Status: Lori Bechtold, Boeing, reviewed the status of VITA 51.2. A four-hour working group meeting was held recently.

VITA 53, Commercial Technology Market Surveillance

Objective: To define the types of market surveillance data needed by DoD program managers in order to develop and implement technology refresh plans.

Status: VITA 53 draft three has been released for comment to the working group. Steve Cecil, CRANE, plans to schedule a conference call in February to discuss any comments. The draft will be revised and submitted to a working group ballot in March.

VITA 55, Virtual Streaming Protocol

Objective: Develop Aurora (serial lite) protocol for XMC and VITA 41.

Status: Andy Reddig, TEK Microsystems, requested that VITA 55 be tabled.

VITA 57.1, FPGA I/O Mezzanine Pin Assignments

Objective: To define a standard mezzanine connector, form factor, and pin assignment strategy optimized for connecting I/O to FPGAs.

Status: VITA 57.1 is an approved ANSI standard currently being revised. When the revisions are complete, an ANSI ballot will be held.

VITA 58, Line Replaceable Integrated Electronics Chassis

Objective: Develop a standard for electronic chassis.

Status: VITA 58 has completed ballot solicitation. The ballot and public review started in January.

VITA 60, Alternative Connector on VPX

Objective: Develop an alternative connector for VPX that is PCB compatible, but not mechanically interoperable.

Status: Colleen Murphy, Amphenol, has released the initial draft and is asking for comments.

VITA 61, XMC with Alternative Connector

Objective: Standardize an alternative connector that is PCB compatible but not intermateable.

Status: Greg Powers, Tyco Electronics, noted that work on the connector is progressing with speeds greater than 6 GHz predicted. Product availability is expected in May.

VITA 62, Power Supply

Objective: Develop a standard for modular power supplies.

Status: The goal of VITA 62 is to define a standard form/fit/function for power supplies to be used in VPX 46.0. The group plans a working group meeting to further define requirements.

VITA 63, KVPX

Objective: Standardize the use of the Hypertronics connector on VITA 46.

Status: The intent of VITA 63 is to provide an alternative connector for specific applications for VPX modules. The connector will have the same PCB layout as the current VITA 46 connector, but will not be intermateable. Production tooling is scheduled for completion in February, and evaluation testing is scheduled for April.

VITA 64, Optimized Footprint for VITA 60

Objective: VITA 60 Optimized Footprint for incorporation of 3U guides and Quick Disconnects (QDs).

Status: Colleen Murphy, Amphenol, discussed the goals of VITA 64 and presented a slide showing the difference between VITA 60 and VITA 64. VITA 64 is similar to VITA 60, but would have narrower guide pins and thus a smaller footprint, allowing a common PCB footprint for all cooling methodologies. The group discussed whether there was a need for both VITA 60 and VITA 64.

VME and Critical Systems / February 2009

VITA Standards Activity Chart

JANUARY MEETING HIGHLIGHTS

Standard *Reaffirmed	Title	Status	*VME and CS* edition
ANSI/VITA 1.0 *2002	VME64 Standards	Released	
ANSI/VITA 1.1 *2003	VME64 Extensions	Released	Aug. 2004
ANSI/VITA 1.3 *2003	9U x 400 mm Format	Released	
ANSI/VITA 1.5	2eSST	Released	Feb. 2004
ANSI/VITA 1.6 *2005	Keying for Conduction-cooled VME	Released	
ANSI/VITA 1.7	Increased Connector Current Level	Released	
ANSI/VITA 3 *2002	Board Level Live Insertion	Released	
ANSI/VITA 4.0 *2002	IP Modules	Released	
ANSI/VITA 4.1 *2003	IP/I/O Mapping to VME64x	Released	
ANSI/VITA 5.1 *2004	RACEway Interlink	Released	
VITA 5.2	RACEway++	Withdrawn	Aug. 2004
ANSI/VITA 6.0 *2002	SCSA	Released	
ANSI/VITA 6.1 *2003	SCSA Extensions	Released	
ANSI/VITA 10 *2002	SKYchannel Packet Bus	Released	
ANSI/VITA 12 *2002	M-Modules	Released	
ANSI/VITA 13	Pin Assignments for HIC on VME	Withdrawn	
ANSI/VITA 17.0 *2004	Front Panel Data Port	Released	
ANSI/VITA 17.1	Serial Front Panel Data Port	Released	Feb. 2004
VITA 17.2	Serial Front Panel Data Port (SFPDP) Channel	Working Group	Feb. 2009
VITA 19.0	BusNet Overview	Withdrawn	
ANSI/VITA 19.1	BusNet MAC	Withdrawn	
ANSI/VITA 19.2	BusNet LLC	Withdrawn	
ANSI/VITA 20 *2005	Conduction-cooled PMC	Released	Apr. 2005
ANSI/VITA 23 *2004	VME64x Extensions for Physics	Released	
ANSI/VITA 25	VISION	Withdrawn	
ANSI/VITA 26 *2003	Myrinet-on-VME	Released	
ANSI/VITA 29	PC•MIP	Released	
ANSI/VITA 30.0 *2005	2 mm Connector Practice on Euroboard	Released	
ANSI/VITA 30.1	2 mm Conduction-cooled Euroboard	Released	
VITA 30.2	Power Connector Equipment Practice	Released	Apr. 2007
ANSI/VITA 31.1	GbE on VME64x Backplanes	Released	Feb. 2004
ANSI/VITA 32	Processor PMC	Released	Feb. 2004
VITA 34	A Scalable Electromechanical Architecture	Working Group	Apr. 2004
ANSI/VITA 35 *2005	Pin Assignments for PMC to VME	Released	
VITA 36	PMC I/O Modules	Withdrawn	Apr. 2004
ANSI/VITA 38	System Management on VME	Released	
ANSI/VITA 39	PCI-X Aux. Std. for PMCs and PrPMCs	Released	Feb. 2004
ANSI/VITA 40	Status Indicator Standard	Released	Dec. 2008
ANSI/VITA 41.0	VXS: VME Switched Serial	Released	Oct. 2006
ANSI/VITA 41.1	VXS: InfiniBand Protocol Layer	Released	Oct. 2006
ANSI/VITA 41.2	VXS: RapidIO Protocol Layer	Released	Oct. 2006
VITA 41.3	VXS: GbE	Working Group	Apr. 2006
VITA 41.4	VXS: PCI Express	Working Group	Apr. 2006
VITA 41.6	VXS: 1X GbE Control Channel Layer	Working Group	Feb. 2009
VITA 41.7	VXS: Processor Mesh Topology	Working Group	
VITA 41.8	VXS: 10 GbE Protocol Layer Standard	Working Group	Oct. 2008
VITA 41.10	VXS: Live Insertion Requirements for VITA 41 Boards	Working Group	Apr. 2006
VITA 41.11	VXS: Rear Transition Modules	Working Group	Apr. 2006

VITA 46.14: Building the industry's first RF backplane interconnect standard

By Robert Normoyle

Historically backplane standards have only defined I/O for digital signals, while many embedded architectures require analog I/O for sensor/exciter interfaces. System design constraints for many applications require that there are no front-panel connectors. Thus, many organizations compromise backplane standards by implementing custom RF interfaces on the user I/O connectors to meet system requirements. This is problematic in many ways including interoperability, upgradability, maintenance, and life-cycle cost. The VITA 46.14 backplane augments the VPX standard to provide RF interconnect on the backplane by defining a mechanical interface and electrical performance specification for an eight-signal RF I/O module.

VITA 46.14 technical challenges

There are many RF I/O module definition technical challenges being researched by the VITA 46.14 standards team, including RF signal performance and mechanical alignment. The initial RF signal performance specifications defined by the draft standard include:

- Frequency range from DC to 26 GHz
- Gain flatness of +/- 1 dB
- VSR of 1.5: 1
- Isolation of 140 dB for HF, 120 dB for V/UHF, and 110 dB for SHF

The isolation requirements, especially at the High Frequency (HF) frequency, are the most challenging of the above RF specifications. Meanwhile, the mechanical challenges of the VITA 46.14 RF module include:

- Insertion alignment
- Insertion/extraction force requirements
- Maintaining good electrical connectivity over many insertions
- Maintaining good electrical connectivity over various environmental conditions

RF module specifications

Tyco Electronics worked with the 46.14 working group on these technical challenges and designed the *VITA 46.14 SMPM RF Module, 8 Position Connector* currently being evaluated (Figure 1). Initial RF performance tests of these connectors – featuring micro miniature blind mate, float mounted cable jack, and mating receptacle – has concluded. The connector's RF performance exceeds the specifications mentioned: The isolation between signal paths is greater than 140 dB for frequencies between 2 MHz to 26 GHz and better than 125 dB isolation from 26 GHz to 40 GHz.

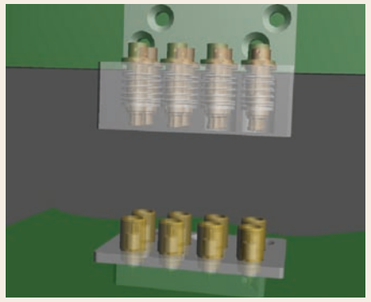

Figure 1

Additionally, the RF I/O module connector for the backplane side is shown as the bottom connector in Figure 1. It hosts eight SubMiniature Push-on Miniaturized (SMPM) connectors that interface to the VPX card's connector shown on top. The RF signals are not routed on the backplane to minimize the amount of digital and system noise coupling to the RF signals. Rather, coax connections are provided for inserting cables on the backside of the backplane. Similarly, the VPX card RF I/O module does not launch the sensitive RF signals onto the motherboard, but instead, it provides a coax connector to launch each signal via coax cable to the end point. This reduces the amount of noise induced upon these signals from digital switching and switching power supplies. The initial plan is to define the VITA 46.14 standard to use RF I/O modules in either or both of the P2 and P6 positions on the backplane. It is envisioned that a VPX architecture requiring RF I/O will have a mix of VITA 46.14 slots and standard VPX slots.

With the superb RF characterization results the working group achieved, we will now move forward with the mechanical testing and writing the standard document. Participation from government and industry is encouraged and welcomed to help ensure that the RF I/O module specification meets a broad range of program requirements. A draft of the standard can be found at www.vita.com.

***Robert Normoyle** is the chief architect in the technology office of DRS-Signal Solutions. For more information on VITA 46.14, email him at Robert.Normoyle@DRS-SS.com.*

Standard *Reaffirmed	Title	Status	*VME and CS* edition
VITA 42.0	XMC	Working Group	Feb. 2009
ANSI/VITA 42.1	XMC: Parallel RIO	Released	Oct. 2006
ANSI/VITA 42.2	XMC: Serial RIO	Released	Oct. 2006
ANSI/VITA 42.3	XMC: PCI Express	Released	Oct. 2006
VITA 42.4	HyperTransport	Working Group	Apr. 2005
VITA 42.6	XMC: 10 GbE XAUI Protocol Layer	Working Group	Dec. 2008
VITA 42.10	XMC: General Purpose I/O	Working Group	
VITA 42.20	XMC: Dual Fabric I/O	Working Group	
VITA 43S	Hot Swap NextGen Mezzanine	Inactive	Feb. 2004
VITA 45S	Serial VME	Canceled	Apr. 2004
ANSI/VITA 46.0	VPX: Base Specification	Working Group	Feb. 2009
ANSI/VITA 46.1	VPX: VMEbus Signal Mapping	Working Group	Feb. 2008
VITA 46.3	VPX: Serial RapidIO on VPX Fabric Connector	Working Group	Oct. 2008
VITA 46.4	VPX: PCIe Mapping and Advanced Switch Signal Mapping	Working Group	Oct. 2006
VITA 46.5	VPX: HyperTransport	Working Group	
VITA 46.6	VPX: GbE	Working Group	
VITA 46.7	VPX: 10 GbE	Working Group	
VITA 46.9	VPX: XMC and PMC User I/O Mapping	Working Group	
VITA 46.10	VPX: Rear Transition Module for VPX	Working Group	Oct. 2008
VITA 46.12	VPX: Fiber Optic Interconnect	Working Group	Oct. 2008
VITA 46.14	RF Interconnects on VPX	Working Group	Feb. 2009
VITA 46.20	VPX: Switch Slot Definition	Working Group	
ANSI/VITA 47	Env., Design and Const., Safety, and Qual. for Plug-in Units	Released	Jun. 2006
VITA 47r1	Revisions to ANSI/VITA 47	Released	Feb. 2008
VITA 47r2	Revisions to ANSI/VITA 47	Working Group	Feb. 2009
VITA 48.0	REDI: Ruggedized Enhanced Design Implementation	Working Group	Feb. 2009
VITA 48.1	Mechanical Specs for Microcomputers Using Air Cooling	Working Group	
VITA 48.2	Mechanical Specs for Microcomputers Using Conduction Cooling	Working Group	
VITA 48.3	Mechanical Specs for Microcomputers Using Liquid Cooling	Working Group	
VITA 49.0	VITA Radio Transport (VRT)	Working Group	Feb. 2009
VITA 49.1	VITA Radio Link Layer (VRL)	Working Group	Oct. 2008
VITA 50	Best Practices for Electronic Module Cooling	Inactive	Dec. 2007
ANSI/VITA 51.0 *2008	Reliability Prediction	Released	Aug. 2008
ANSI/VITA 51.1 *2008	Reliability Prediction: MIL-HDBK-217 Daughter	Released	
VITA 51.2	Physics of Failure Reliability Predictions	Working Group	Feb. 2009
VITA 52	Lead-free Practices	Working Group	Oct. 2006
VITA 53	Commercial Technology Market Surveillance	Working Group	Feb. 2009
VITA 54	Embedded Platform Management Architecture (EPMA)	Inactive	Aug. 2005
VITA 55	Virtual Streaming Protocol	Inactive	Feb. 2009
VITA 56	Express Mezzanine Card (EMC)	Inactive	Oct. 2007
ANSI/VITA 57 *2008	FMC: FPGA Mezzanine Card Standard	Released	Dec. 2008
VITA 57.1	FPGA I/O Mezzanine Pin Assignments	Working Group	Feb. 2009
VITA 58	Line Replaceable Integrated Electronics Chassis	Working Group	Feb. 2009
VITA 59	RSE: Rugged System-On-Module Express	Working Group	Dec. 2008
VITA 60	Alternative Connector on VPX	Working Group	Feb. 2009
VITA 61	Alternative Connector for XMC	Working Group	Feb. 2009
VITA 62	Power Supply Modules	Working Group	Feb. 2009
VITA 63	KVPX	Working Group	Feb. 2009
VITA 64	Optimized Footprint for VITA 60	Working Group	Feb. 2009

For corrections or suggestions, contact Chris Ciufo, *VME and Critical Systems* magazine, at cciufo@opensystemsmedia.com.