The evolution of Eurocard

By Justin Moll

Editor's Note: In January 2006 at the Bus&Board Conference, Justin gave a presentation on the evolution of backplanes. This article will cover many elements from the presentation and include other related technology advances.

Backplane-based architectures have advanced and continue to advance to meet market needs. We'll take a look at the evolution of many of the VITA and PICMG-based architectures, see where they fit today, and analyze some upcoming technologies.

Origins of Eurocard and VME

The VERSAbus by Motorola in 1979 based on the 68000 microprocessor formed the electrical basis for the new VMEbus (Versa Module Eurocard), along with the preexisting Eurocard mechanics.

The VMEbus was created in 1981 as a result of the joint efforts of Motorola, Philips/Signetics, and Mostek. Subsequently, it was adopted as a standard by IEEE (IEEE 1014-1987) and IEC (IEC 60821). At the time, the VMEbus was a 16-bit, easily upgradeable, microprocessor independent, nonproprietary bus standard with a proven mechanical form factor.

As technology progressed with faster boards and chips, the necessity to upgrade from 16 bit, 40 MBps to 32-bit (3U) and 64-bit (6U) with twice the bandwidth (80 MBps) caused the VMEbus specification to be revised through IEEE 1014-1987 and ANSI/VITA 1-1994. The latter is also referred to as *VME64*. This improvement, along with an automatic plug-and-play feature, auto slot ID, and many others, served to enhance the popularity of VMEbus in embedded applications.

VME became very popular, but bandwidth and I/O constraints started to become a problem in applications where more performance was required. So, ANSI/VITA 1.1-1997, also called *VMEbus Extensions* or *VME64x*, added new capabilities including a new 160-pin connector, a 95-pin P0/J0 connector for additional I/O, 3.3 V power plane, 160 MBps bandwidth, more 5 V power, rear plug-in units, and EMC front panels with injector-ejector handles and geographical addressing. VME64/64x has also proven to be an unqualified success in Air Transport Rack (ATR) type enclosures with conduction cooling per IEEE 1101.2.

By 1997-1998, Elma Bustronic Corp., in cooperation with Arizona Digital, released another improvement to the speed of the VMEbus – the VME320. VME320 has a data transfer rate of 320 MBps using a star interconnection scheme.

Later, we'll look at how switched fabrics are changing the game. First, we'll discuss VME's nemesis, CompactPCI.

CompactPCI

About the same time the VME320 was created, a new bus-based architecture, *CompactPCI*, was born. It was based on the 2 mm HM connector standard and the IEEE 1101.10/11 mechanicals with PCI being the core electrical portion. PCIbus was a proven bus with an enormous installed base in different market segments such as telecom, industrial automation, and others. The CompactPCI architecture could also leverage off the lower-cost, widely available PCI silicon WinTel (Windows/Intel) architecture, rapidly improving performance. A 64-bit implementation could boast a data transfer rate of 533 MBps. CompactPCI was created by a group of PCI manufacturers under PICMG.

With a soaring demand for more speed and bandwidth fueled by the Internet boom, CompactPCI became extremely popular with its open standard that helped speed time to market for the telecom arena. The Eurocard form factors of 6U x 160 mm for front line cards and 6U x 80 mm for rear transition cards were tailor-made for platform providers to develop rackmount equipment that met the NEBS criteria for 300 mm depth as well as cable management. However, as faster processors emerged over time, it was clear that CompactPCI would need changes to compete in higher-end applications.

Backwards-compatible switched fabrics – PICMG 2.16/2.17/2.20

Eventually, the slot limitations of CompactPCI and the bottlenecks to higher data transfer rates prompted the foray into switched fabric architectures such as PICMG 2.16 (cPSB), 2.17 (StarFabric), and 2.20 (Serial Mesh). CompactPCI is limited to eight slots at 33 MHz and five slots at 66 MHz. Compact Packet Switching Backplane (CPSB) was the first and the most successful. Since these were all based on the PICMG core 2.0 CompactPCI specification, the form factor remained 6U x 160 mm (Eurocard). The specification took undefined portions of a standard CompactPCI backplane and assigned pinouts for the fabric. Switch slots, which run the fabrics, were new. Otherwise, the backplane slots had the same form factor and accepted legacy CompactPCI cards.

The CompactPCI buses on the backplanes are still limited to eight loads (at 33 MHz); not all slots need to implement the CompactPCI bus on a PICMG 2.16 or 2.17 backplanes. Also, low-profile bridges allow more CompactPCI slots without interfering with rear I/O. However, the bridges still occupy a load in each segment. The performance of PICMG 2.16 is approximately up to 830 Mbps slot-to-slot, where standard CompactPCI accommodated approximately 266 MBps (64-bit at 33 MHz).

Backwards-compatible switched fabrics – VITA

VME has likewise integrated switched fabrics into technology. GbE over VME adds switched fabric performance to the VME64x backplane. The specification takes the previously undefined portion of the backplane in the P0 section and defines the pin-outs for a GbE fabric routing. The new feature of the backplanes is switch card slots that drive the fabric. Otherwise, the backplanes are fully backwards compatible. This provides the ability to have data traffic at high speeds in one *plane* of the backplane and have the control functions of VME in another *plane*.

However, as new applications and capabilities arose, it became apparent that the 2 mm HM connector in CompactPCI and the P0 section of VME64x had its limitations. Thus, the VXS (VME Switched Serial) specification uses a new high-speed connector. VXS is basically the same concept as GbE over VME, except it uses the MultiGig RT-2 connector. Where the 2 mm HM started to see performance problems above approximately 1.3 Gbps, the MultiGig claims to perform above 6 Gbps. VXS also is fabric-agnostic: Fabrics such as InfiniBand, Serial RapidIO, Gigabit Ethernet, and so on, can be implemented. The performance of VXS is approximately up to 3,000 Mbps slot-to-slot.

Although the new P0 connector in VXS is not backwards compatible, many VME64x cards do not use the P0 connector, and the backplane can always be designed to have legacy VME64x slots (see Figure 1, which depicts a VXS processor mesh). In 2005-2006, Elma Bustronic created a new technology called VXS *processor mesh* (VITA 41.7). It adds a mesh fabric to VXS. The bandwidth is approximately up to 5,000 Mbps slot-to-slot.

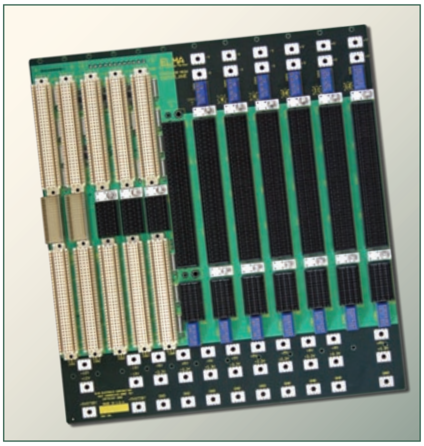

Figure 1

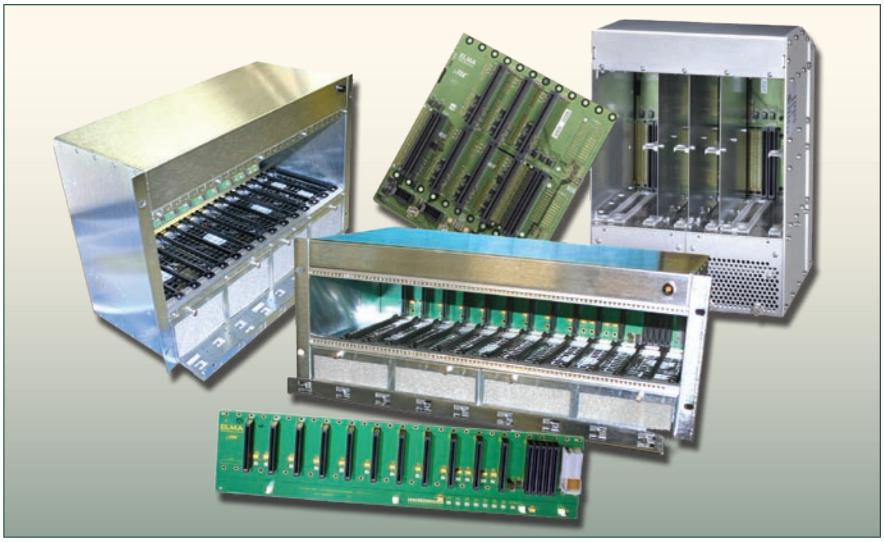

Figure 2

Non-backwards-compatible fabrics – PICMG (AdvancedTCA, MicroTCA)

In late 2001, PICMG formed a committee to develop a new series of telecom specifications: PICMG 3.0 Advanced Telecom Computing Architecture (AdvancedTCA) calls out for an 8U x 280 mm front boards and 6U x 60 mm rear boards.

AdvancedTCA was designed not to be backwards compatible with CompactPCI; it is a whole new form factor – geared toward the central office applications. AdvancedTCA has the following features aimed specifically at the central office:

- 8U x 280 mm boards, with wider 1.2" spacing
- 48 Vdc as the sole power delivered to boards (most CO systems use that voltage exclusively)
- Serial interconnects for bandwidth
- Flexible user I/O
- Mandatory shelf management based on IPMI
- High level of service reliability (5-nines or more) from integrating features for redundancy, serviceability, and manageability
- Low-cost sheet metal solution (in high volumes)

Using the ZD connector rated at 5 Gbps and with dual star, mesh, or replicated mesh topologies, AdvancedTCA has a huge bandwidth improvement over CompactPCI. The performance is approximately 5,000 Mbps slot-to-slot.

MicroTCA was developed as a smaller, cheaper architecture based on the AdvancedTCA concept. It reduces size and cost by eliminating the AdvancedTCA carrier, enabling AdvancedMC modules to be plugged directly into the backplane. MicroTCA provides scalable bandwidth from 1-40 Gbps and scalable availability ranging from 3-nines (99.9 percent) to 5-nines uptime (99.999 percent).

The MicroTCA Carrier Hub (MCH) provides interconnect, power conversion, clock distribution, and system management functionality needed to support up to 12 AdvancedMC modules. MicroTCA's high performance and low power consumption make it a good fit for wireless base stations, digital loop carriers, optical ADMs, enterprise networking, storage servers, and nonrugged mil/aero communications. Figure 2 depicts various MicroTCA products. Like AdvancedTCA, performance is approximately 5,000 Mbps slot-to-slot. To offer advanced performance but maintain some compatibility with legacy VITA and PICMG standards, some new hybrid technologies have also been developed.

New hybrids

Hybrids are what can be called *partially* backwards compatible. One could use the legacy technology, but that requires a bit more changes than the fully backwards-compatible technologies. One of the *hybrids* is CompactPCI Express.

Similar in concept to VME's VXS, CompactPCI Express uses a new connector to overcome performance limitations of 2.16/2.17. A new ZD connector rated at 5 Gbps and using the PCI Express fabric, the performance of CompactPCI Express is vastly increased while maintaining some backwards compatibility. The support of legacy 32- or 64-bit CompactPCI boards is accomplished by a PCIe-to-PCI bridge. The use of CompactPCI boards of 33 MHz, 66 MHz, or 133 MHz is possible. CompactPCI Express utilizes a serial point-to-point bus with a read-only bandwidth up to 16x 2.5 Gbps or 8x 2.5 Gbps full duplex bandwidth. Providing support for several different card form factors with connectivity in 1x, 2x, 4x, and 8x increments, each link represents one full duplex 2.5 Gbps interconnect path. Because the CompactPCI Express architecture continues to support the P3, P4, and P5 in all 6U slot types, CompactPCI Express can continue support for all existing CompactPCI secondary architectures such as PICMG 2.5, 2.20, 2.16, 2.17, and 2.18. They can be used as either functions on native CompactPCI Express cards or as legacy cards in the original CompactPCI format.

VPX (VITA 46/48) is another hybrid where some backwards compatibility is possible. The technology is highly customizable and most backplane designs will be custom as the routing is highly undefined. This allows a lot of flexibility but a less straightforward *follow step A to step B* approach. VPX comes in 3U and 6U versions, and the chassis can be convection cooled (forced air), conduction cooled, or liquid cooled. V48.3 is the most aggressive version with special modules for liquid flow-through cooling. On the backplane, the key difference is it offers a mesh configuration and the VMEbus is optional. The aggregate bandwidth slot-to-slot is approximately 5,000 Mbps (Figure 3).

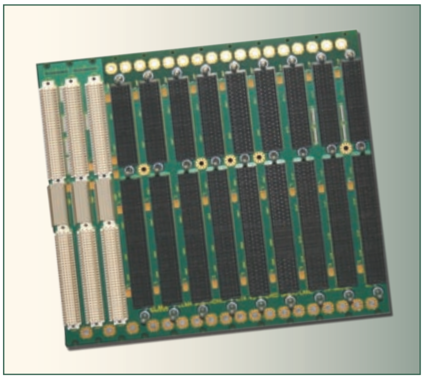

Figure 3

VXS processor mesh in simplest terms is a mesh VXS backplane. Processor mesh allows backwards compatibility to VXS and legacy VME64x slots and has a control plane and central I/O slot. Many ask what the difference is between processor mesh and VPX. Figure 4 shows a comparison between VXS (including processor mesh) and VPX.

Other new hybrids include Industrial PCI Express and serial mesh. Figure 5 shows a comparison of the features of the newer architectures.

A question of backwards compatibility

One of the key elements in Eurocard is the question of backwards compatibility. The industry has developed specifications that have tremendous performance in maintaining a partial or full backwards-compatible premise. Backplane architectures such as legacy VME and CompactPCI are still going strong. The hybrids will also help preserve the investment in these technologies and keep them an important part of the industry product mix. The completely new specifications such as AdvancedTCA offer their own set of advantages along with high bandwidth. But the backwards-compatible specs are catching up in performance. Will it be too late for architectures such as CompactPCI Express, which got going a little late? We will have to wait and see. Ω

Justin Moll *has more than 10 years of high-tech marketing and sales experience and has been with Elma Bustronic and Elma Electronic Inc. since 2000. As the director of marketing for Elma Bustronic and manager of PR for Elma Electronic, he has been a key figure in the strategic marketing for both companies. Justin is active in VITA and PICMG and has been the VP of marketing for the StarFabric Trade Association since 2003. His previous positions include marketing services manager for E21 Corporation and account manager for Elcon Products International, now a Tyco Electronics company. Justin received his BS degree in Business Administration from the University of California, Riverside.*

For more information, contact Justin at:

Elma Bustronic
44350 Grimmer Blvd.
Fremont, CA 94538
Tel: 510-656-3400
E-mail: JMoll@bustronic.com
Website: www.elmabustronic.com

	Slot-to-Slot Bandwidth (Mbps[1])	Form Factor(s)	Slot Limitations (19" rack)	Voltages (typical)	Cooling options (typical)	Rear I/O	Slot Pitch	Signal Connectors
VXS Processor Mesh (VITA 41.7)	7500	6U x 160 mm	16	3.3 V, 5 V, 12 V	Convection, conduction	6U x 80 mm	1.0"	MultiGig RT-2[5]
AdvancedTCA (PICMG 3.0)	7500	8U x 280 mm	14	48 Vdc[3]	Convection	8U x 70 mm	1.2"	ZD
VXS (VITA 41)	5000	6U x 160 mm	21[2]	3.3 V, 5 V, 12 V	Convection, conduction	6U x 80 mm	0.8"	MultiGig RT-2[5]
VPX (VITA 46)	5000	3U or 6U x 160 mm	16	5 V, 12 V, 48 V	Convection, conduction, or liquid	6U x 80 mm	0.8" or 1.0" (liquid cooled)	MultiGig RT-2[5]
MicroTCA (MicroTCA.0)	5000	75 mm or 150 mm x 180 mm	29	48 Vdc	Convection	none	0.6", 0.8", or 1.2"	AdvancedMC
CompactPCI Express (EXP.0)	5000	3U or 6U x 160 mm	16[6]	3.3 V, 5 V, 12 V	Convection	6U x 80 mm	0.8"	2 mm HM, ZD
cPSB (PICMG 2.16)	833	6U x 160 mm	21[4]	3.3 V, 5 V, 12 V	Convection	6U x 80 mm	0.8"	2 mm HM

1 Assumes 1 pair = 2.5 Gbps
2 Max is 20 VXS, if one slot legacy VME64x then 21
3 AC is possible
4 CompactPCI bus is limited to 8 slots @ 33 Mhz
5 Possible to also use 160-pin DIN
6 16 x1 slots or more slots with on board switch as defined in the base specification

Figure 5

	VITA 41	VITA 46
Form factors	6U	3U, 6U
Performance maximum (theoretical)	Star/Dual Star: 30 Gbps Processor mesh: 112 Gbps	112 Gbps
Topologies (typical)	Star, Dual Star (payload mesh and processor mesh also offered)	Mesh
Cooling mechanicals	Convection (IEEE1101.10/11) Conduction (IEEE1101.2)	46.1: Convection (IEEE1101.10/11) 46.2: Conduction (IEEE1101.2) 46.3: Liquid Flow Through
Electrical architecture	VME64x Serial fabric System management	VME64x Serial fabric System management
Signaling protocols	VME, IPMI, I2C Ethernet, Serial RapidIO, PCI Express	VME, IPMI, I2C Ethernet, Serial RapidIO, PCI Express
Backward compatibility	VME, VME 64, VME64x, IEEE 1101.2, VITA 48 PMC, XMC, VITA 56 (only on payload cards)	Not direct, but hybrid interface defined IEEE 1101.2, VITA 48, PMC, XMC, VITA 56
Minimum payload defined	2 channels	N/A
Fixed slot signal assignments	Yes	No
Slot pitch	0.8" payload slots/0.8" or 1.0" for switch slots	0.8" for convection or conduction cards 1.0" for liquid cooled
User I/O	Switch – 18 payload channels, 4 interswitch channels, 2 reserved channels + 121 additional single-ended signals (15 permanently assigned to system utilities) Payload – 2 fabric channels + 30 single-ended signals and 5 single-ended signals permanently assigned to system utilities	Flexible assignment of connectors for either single-ended or differential use Assignment to fabric or I/O depends is never fully defined. See maximum channels.
Connector System Backplane Connector System Daughtercard	Switch – 9-column – MultiGig backplane connector, 12-column – MultiGig daughtercard connector Payload – 9-column – MultiGig backplane connector, 7-column – MultiGig daughtercard connector	9-column – MultiGig backplane connector 7-column – MultiGig daughtercard connector
Maximum channels*	Switch – 192 total differential pairs/24 bidirectional 10 Gbps channels (assuming 2.5 Gbps per pair) Payload – 16 differential pairs/2 bidirectional 10 Gbps channels (assuming 2.5 Gbps per pair)	6U – 192 total differential pairs or 24 bidirectional 10 Gbps channels (assuming 2.5 Gbps per pair) 3U – 64 total differential pairs or 8 bidirectional 10 Gbps channels (assuming 2.5 Gbps)
Keying and coding	Guide pin with integral key and separate IEC 61076-4-101 key	Tyco MultiGig Guide pin and integral key
Voltages required	5 Vdc – VXS 5, 3.3, +12, -12 Vdc – VME for VME-enabled payloads	All optional: 5 , 12, or 48 Vdc
Current announced product	32 boards	3 boards
Released documents (or ready to be sent to ANSI for approval)	41.0 Core 41.1 InfiniBand 41.2 Serial RapidIO 41.10 Live Insertion 41.11 Rear Modules	46.0 VPX Core 46.1 VME on P1
Draft documents	41.3 Gigabit Ethernet 41.4 PCI Express 41.5 Aurora 41.6 Processor 41.7 Control Plane	46.3 Serial RapidIO 46.4 PCI Express 46.5 HyperTransport 46.9 XMC PMC 46.10 RTM

*The number of I/O channels indicated is based upon the total number of differential pairs defined in the two base standards (VITA 41.0 and 46.0). The subsidiary documents assign these differential pairs to various uses so users should consult the specific subsidiary implementation to determine how the differential pairs may be used.

Figure 4