Hybrid VPX backplanes bridge legacy systems

By Melissa Heckman

You may have heard that VITA 46 – also known as *VPX* – offers tremendous next-generation I/O potential and high-speed serial fabrics. What you may not know is that while VPX is radically different from VME, hybrid backplanes can bridge the two standards.

VPX is a new high-performance VME architecture using switched serial fabrics, typically in a mesh topology that offers tremendous bandwidth potential. While different from the traditional VME64 P0/P1/P2 backplane architecture, VPX can be compatible with legacy systems in "hybrid" backplanes. The author examines the architecture and nuances of making next-generation VPX boards interoperate with legacy VME systems via hybrid backplanes.

Hybrid VPX backplane

First, let's take a look at VPX versus VME64x backplanes. VME64x uses the VME parallel bus across a 160-pin DIN connector. VME64x's slot-to-slot bandwidth is approximately 80 MBps. VPX's slot-to-slot bandwidth is approximately 5,000 MBps. The VME connectors are ideal for single-ended signals, but the VPX architecture uses the wafer-based MultiGig connector with much greater bandwidth and supports either differential or single-ended signals. One of the main differences is that VME64x has only 110 undefined pins available in the J1/J2 connectors and 205 pins total if you include the 95 P0 pins. However, VPX has 480 pins per slot that could be assigned by the user or they could be used as up to 186 differential pairs. This is because the connectors J1-J6 have no required (defined) use. The backplane in Figure 1 shows the physical differences of the connectors. With a robust high-speed differential connector and direct point-to-point mesh connections, VPX allows much higher performance than VME64x. However, real-time determinism of VME64x, along with its mature and well-understood architecture, vast product ecosystem, and backwards compatibility to legacy VME (such as VME32 and earlier) has its advantages. VPX and VME64x together can be a powerful combination.

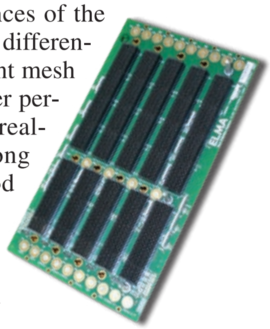

Figure 1

As stated in section 1.2 of the VITA 46 specification: "The dot specifications allow the use of the single-ended connector allocation for parallel buses, such as VME or PCI, completing the compatibility between older standards and this one." In other words, buses like VME can be given a pinout allocation to run the bus across the VPX slots. Using the VMEbus is more intuitive than, say, the PCI bus found in other embedded systems. First, many of the applications in which VPX is expected to be used are ones where VME is already commonly used: rugged, military, Eurocard, real-time, and so on. Of course, VPX is aimed at the very high-end applications where VME alone just isn't enough. In particular, applications with vast amounts of data processing, imaging, and the like are key areas. Further, the VITA 46 VPX specification is coming from the vendors that largely use VME such as Mercury Computer Systems, Inc. and Curtiss-Wright Controls Embedded Computing. It is similar in many ways to the fabric-centric VITA 41 VXS specification, which also stems from the VME community.

There are many benefits to having some compatibility with VME. It saves time and costs in software rewriting, reuse of drivers, as well as hardware. There are savings in terms of costs and training/learning curves in reusing legacy cards. Many users in the same mil/aero key market are highly familiar with VME. Hybrid systems supporting VME/VPX may make some customers more comfortable with the move to VPX. It sounds funny, but it's amazing how VME can give a customer that "warm, fuzzy feeling." This, of course, is a testament to VME's longevity and success in applications and military programs that run for 10 years or more.

Design flexibility

One compelling feature of VPX is that it has a lot of design flexibility. The architecture can simultaneously support a mix of bus segments including full mesh, pipeline, or single or dual star topologies. Connector segments J1 to J6 can even be implemented for either differential signals or single-ended signals. The architecture offers design flexibility as opposed to a more fixed and defined architecture. This allows a user to use exactly as many pins, connection configurations, and so on, as are needed for the specific application. VPX designs a standard card layout and standard mechanics but lets system engineers connect the dots between them so as to conform to the exact needs of their requirement. But in order to understand VPX hybrids deeper, we need to look at the topology.

Topology

To understand the topology of VPX, let's first look at a typical mesh VPX backplane (see Figure 1 on page 20 for a five-slot version). All of the slots use the Tyco MultiGig RT-2 high-performance connector. In this particular topology, there are no slots nor connections for the VMEbus. Legacy VME cards cannot be plugged into this backplane. The connections are illustrated in Figure 2.

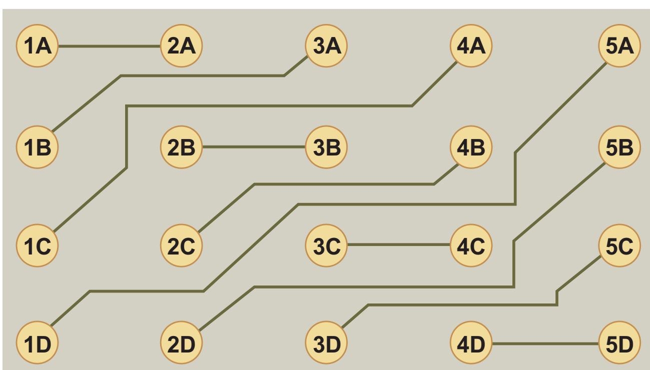

Figure 2

Now, let's take a look at a 12-slot hybrid backplane with nine VPX slots and three legacy VME64x slots (see Figure 3). The routing is very similar for the mesh configuration. However, pins are now allocated for the VMEbus. (See Figure 4 for an illustration of the backplane connections.) The VPX slots are split into two clusters that are connected in a ring to Slot 4. Slot 4 is bused to the three VME64x slots.

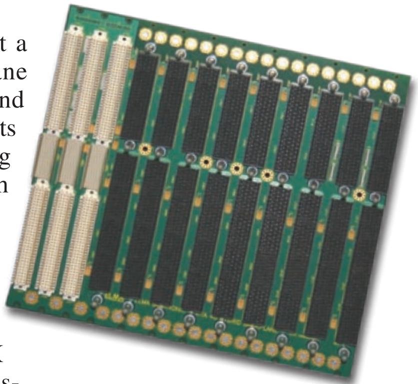

Figure 3

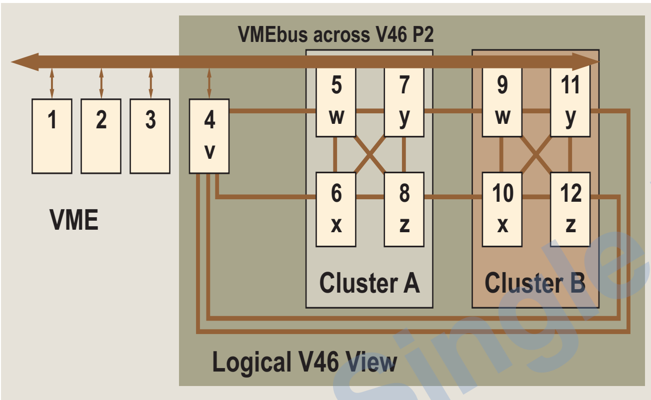

Figure 4

Now, let's take a look at a VPX board with VMEbus implementation. The 185 board from Curtiss-Wright Controls Embedded Computing is one example. As illustrated in the pinout in Figure 5, the board reserves pins for VMEbus signals. Note that this P0 pinout reflects the 6U 12 V high-voltage prime-power case, as the power options are a little different than for 3U or if the high-voltage prime power was 48 V. Also, some of the terms may have changed since the pinout chart was created. The flexibility of VPX and products like these allows a wide range of VPX/VME implementations.

One consideration that needs to be reviewed closely in developing any VPX backplane (hybrid or not) is the type of backplane material that is used.

Backplane materials

With 205 pins in each slot for VME64x (including the 96 on P0) and 480 for VPX with up to 186 differential pairs – the result is an incredible amount of I/O to route around a PCB-based hybrid backplane. Additionally, VPX adds high-speed differential serial signals that can switch well in excess of 3.0 GHz. The VITA 46 spec acknowledges that the backplane may require up to 16 routing layers and *a huge 36-layer PCB*. So it seems that no ordinary PCB-based hybrid backplane can accomplish these challenging technical tasks (massive I/O at microwave frequencies). The key to making a hybrid VME/VPX backplane work is the PCB material and layer stack-up.

In short, the backplane designer should do simulations to optimize the signal quality of the design and minimize the negative stub effects. One key method is to take the performance requirements, which typically would be 3.125 GBps or 6.250 GBps and route the backplane to minimize the layer count, but follow proper design rules. Design rules typically specify how close signals should be to another or to components, avoiding 90 degree bends of the signal, and so on. Reducing the layer count can shorten the stubs, thus reducing the stub effect. In most cases, a high-grade laminate will need to be used – even in smaller (fewer slot) backplanes. For example, the five-slot VPX backplane in Figure 1 uses an FR-408 low-dielectric material. VPX backplanes typically have too many layers to use standard FR-4 PCB material, that is, if you wish to use signals that exceed speeds of 3.125 Gbps. Backdrilling the vias is another option. Of course, either of these methods raises the cost of the backplane. **CS**

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Backplane P0 Connector

	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	12V_Vs1	12V_Vs1	12V_Vs1	NC_P50_D1	12V_Vs2	12V_Vs2	12V_Vs2
2	12V_Vs1	12V_Vs1	12V_Vs1	NC_P50_D2	12V_Vs2	12V_Vs2	12V_Vs2
3	5V_Vs3	5V_Vs3	5V_Vs3	NC_P50_D3	5V_Vs3	5V_Vs3	5V_Vs3
4	SM2	SM3	GND	12VNEG_Aux	GND	VME_SYS_RST_L	NVMRO
5	VME_GAP_L	VME_GA_L4	GND	3V3_Aux	GND	SM0	SM1
6	VME_GA_L3	VME_GA_L2	GND	12VPOS_Aux	GND	VME_GA_L1	VME_GA_L0
7	TCLK	GND	TDO	TDI	GND	TMS	TRST_L
8	GND	REF_CLK_N	REF_CLK_P	GND	RES_BUS_N	RES_BUS_P	GND

Figure 5