

VITA 46.9: Ensuring mezzanine I/O pinout interoperability for VPX and VPX-REDI

By *Jing Kwok*

The emerging VITA 46 (VPX) and VITA 48 (VPX-REDI) bus architecture standards are bringing new life – and faster speeds – to high-performance processing configurations previously untouchable to legacy VME systems. They also provide more I/O pins, giving more freedom in I/O definition to system integrators; however, this increased freedom can result in mezzanine/baseboard incompatibility issues for end users. Now VITA 46.9, a subsidiary specification of VPX, steps into the front line by solving XMC and PMC I/O mapping issues and increasing interoperability among vendors.

The VITA 46 (VPX) family of standards defines an embedded computer module that builds on the utility of the VMEbus Eurocard form factor by providing a series of high-speed, fabric capable backplane MultiGig RT-2 connectors, in lieu of the conventional DIN pin and socket connectors. Proper use of these connectors for a variety of backplane signaling standards is defined further in the VPX “dot” subsidiary specifications. These “dot” standards dictate the type of connector populated at each allowable location on a VPX card and the interface signal mappings of the different serial fabric options.

VPX cards, like earlier VME boards, will typically provide mezzanine card installation sites for the addition of application-specific functions. PCI Mezzanine Card (PMC) and/or Switched Mezzanine Card (XMC) mezzanines may be optionally installed on the VPX card, depending on the functionality designed into the base plug-in module or “carrier” by the designer. VITA provides several standards for bus signaling on PMC and XMC cards

to ensure interoperability among board vendors. These standards also define the “user I/O” connector contacts that are available to the mezzanine card designer. VITA 46.9 is one such standard, defining the differential pairs to be used in mapping mezzanine I/O to the VPX backplane connectors.

VITA 46.9 to the forefront

In the past, the failure to define the consistent usage of I/O pins has created problems resulting in mezzanine cards that were incompatible with certain baseboards. In the VME specification, I/O signals for the VME P0 and P2 were only defined for single-ended configuration. Single-ended signaling is typically used on PMC mezzanine cards to address common I/O interfaces that do not require tightly controlled signal environments. Consequently, differential I/O signals were left undefined, which encouraged different vendors to use different pinout schemes. This resulted in a variety of problems for end users. For example, in some cases mezzanine cards would only

work with certain specific baseboards. Also, in some cases, mezzanine modules required different layouts depending on whether the module was to be installed in the baseboard’s PMC site 1 or in site 2. One layout would be needed to match P0 and a different one to match P2.

The VPX working group, armed with knowledge of past problems resulting from the lack of definition for differential I/O signals for VME P0 and P2, decided to eliminate the confusion experienced by earlier VME users and solve the problem by defining differential I/O pinout in the VPX specification. The alternative might have resulted in the emergence of numerous competing I/O options that could hamper interoperability.

The VPX working group, to address this problem, has created the VITA 46.9 “dot-spec,” which defines the standard differential pairs to be used for mapping mezzanine I/O to the VPX backplane connectors. The working group also ensured that the resulting differential

Advantages of VPX over legacy VME

While VME has long been the bus architecture of choice for military and aerospace applications, recent advances in technologies, particularly in interconnects, have demonstrated the need for an advance in system development. The new VPX (VITA 46) and VPX-REDI (VITA 48) bus architecture specifications update the VMEbus legacy to provide support for high-speed switched serial fabrics, such as Serial RapidIO (SRIO) and PCI Express, and support distributed processing at speeds and in network configurations unreachable by VME64x.

One of the key advantages of VPX over legacy VME is the greater number of I/O pins that it makes available to end users. This gives integrators the freedom to define I/O as they need to add market differentiation and meet the require-

ments of unique applications. The increased backplane I/O provided by VPX also makes it possible for some of these extra I/O pins to be allocated to additional XMC and PMC card I/O. This is in contrast to VME and some other newer standards that provide only limited backplane I/O.

In fact, VPX is the only bus architecture format that defines a standard approach for XMC I/O to the backplane. VPX offers another benefit to XMC module users resulting from its use of Tyco’s MultiGig RT-2 connectors, greatly improving signal integrity for rear-panel mezzanine I/O compared to VME or CompactPCI connectors. Also, the XMC Pn6 connector provides superior performance to the PMC Pn4 mezzanine connector because standard mapping provides intervening grounds and significant physical separation between pairs.

pinout mapping would be symmetrical, for example, work on either a 6U VPX P3/4 set or on a P5/6 set. In addition, the working group also defined differential pinout usage for 3U VPX cards and their P1/2 set. The result is that VITA 46.9 solves XMC/PMC I/O mapping on VPX and ensures and greatly simplifies the interoperability of basecards and mezzanine I/O cards from different vendors.

“VITA 46.9 ensures interoperability while providing flexibility by offering a number of standard combinations.”

Innerworkings of VITA 46.9

The objective of the VITA 46.9 standard is to supplement the VITA 46.0 base standard to fully define the user I/O signal mapping between the pins of PMC and/or XMC card sites provided on a VPX compliant carrier for both 3U and 6U modules. In addition, it defines the fabric mapping for a 3U module and placement for two channels of GbE 1000BASE-T. VITA 46.9 ensures interoperability while providing flexibility by offering a number of standard combinations. The following combinations were determined the most likely to be actually implemented in practice:

- PMC Jn4 assigned to 3U V46-P2 differential and single-ended connector
- XMC Jn6 assigned to 3U V46-P2 differential connector
- PMC Jn4 assigned to 6U V46-P3, 5 differential connector
- XMC Jn6 assigned to 6U V46-P3/4, 5/6 differential connector

To accommodate this, various mapping patterns have been defined:

- **P64s** – Maps all 64 contacts of PMC-Jn4 to VPX differential wafers.
- **X12d** – Maps 12 selected differential pairs of XMC-Jn6 to VPX differential wafers.
- **X20d24s** – Maps all 20 differential pairs of XMC-Jn6 and 24 single-ended pairs to VPX differential wafers. This pattern fits within one VPX connector.

- **X20d38s** – Maps the entire XMC connector to VPX differential wafers. This consists of all 20 differential pairs of XMC-Jn6 and all 38 single-ended signals.

For 6U cards, several overall configurations can be accommodated by selecting from the previously defined mapping patterns (see Figure 1):

- VPX P3/P5 mapped to PMC Jn4 using the P64s and P4/P6 mapped to the XMC Jn6 using the X12d pattern
- VPX P3/4, P5/6 mapped to XMC Jn6 using the X20d38s pattern

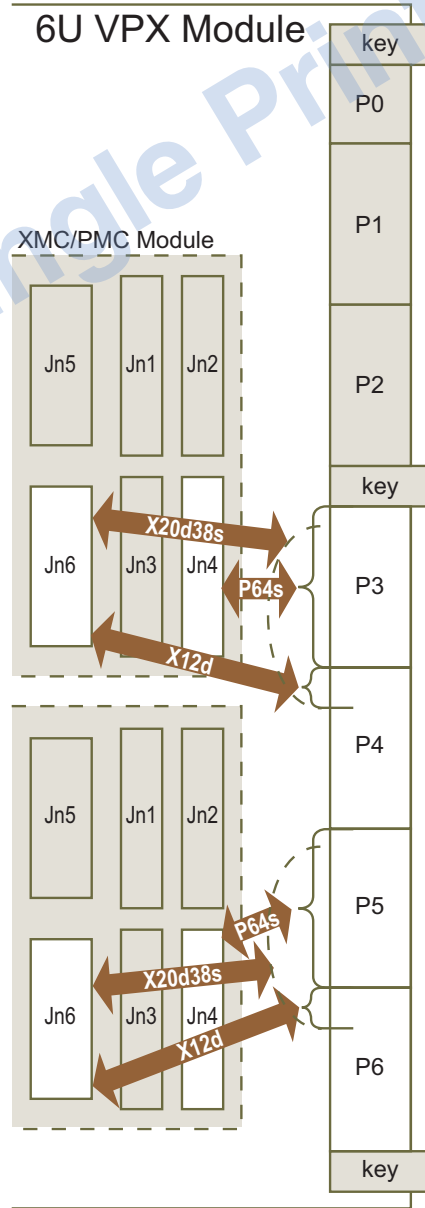


Figure 1

For 3U cards, the following configurations are supported, as shown in Figure 2:

- VPX P2 mapped to PMC Jn4 using the P64s and P1 mapped to the XMC Jn6 using the X12d pattern
- VPX P2 mapped to X20d24s

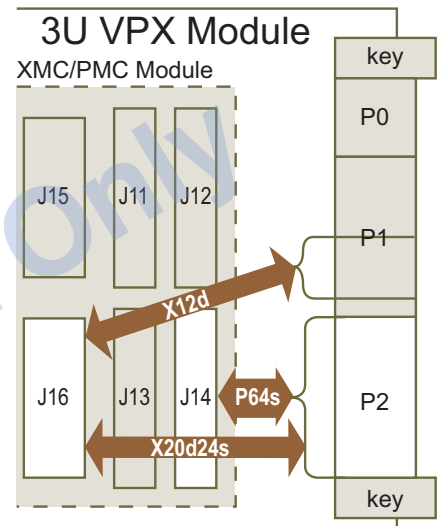


Figure 2

Figures 1 and 2 both show all configurations mapped on a carrier card. However, in practice, only one configuration will be mapped at a time. For example, a VPX carrier card that supports only a PMC mezzanine will only use the P64s mapping as it will only have Jn4 installed. For a VPX carrier card that supports only XMC Jn6, then the X20d38s mapping will be used in the 6U case and the X20d24s mapping will be used in the 3U case. For a VPX carrier card that supports both XMC Jn6 and Jn4, then P64s and X12d would be mapped.

VITA 46.9 mapping patterns explored

The mapping pattern P64s is relatively straightforward. The P64s maps the 64 Jn4 I/O pins on a PMC mezzanine to the VPX RT2 connector. The 64 pins are arranged as two rows of 32 pins each. One column is labeled odd and the other even. In selecting the differential pairs, the working group selected pins next to each other as differential pairs. That is, pins 1-3 are considered a differential pair and pins 2-4 are considered a differential pair. This approach was taken to ease matched length routing on the PMC module and the carrier card. These pins are then mapped to the VPX RT2 connector.

The mapping pattern X12d was a more complex challenge. The X12d maps 12 differential pairs of the XMC Jn6 connector to the RT2 connector. The working group chose 12 differential pairs as a good tradeoff between the amount of XMC I/O mapped to the MultiGig RT-2 connector versus the number of I/O lines left over for use by the host card itself. The working group spent much time debating this mapping. The main issue was which 12 pairs should be mapped? The XMC Jn6 connector is an open field connector arranged as 6 columns (A to G) and 19 rows of pins, for a total of 114 pins. Much signal integrity work was done in the XMC working group. It showed that 20 differential pairs can be obtained by placing them on the odd rows on columns AB, DE with grounds on the even rows of those same columns. The XMC working group further defined that rows 1,3,5,7 were to be transmit lines and 11,13,15,17 were to be receive lines. This approach provides an XMC mezzanine card with the ability to support up to eight lanes of serial tx/rx traffic. The working group decided to stay with this pattern and allowed 8 differential pairs for a fabric port on rows 1,3 and 11,13 and assigned the remaining 12 pairs for the X12d backplane I/O pattern.

The patterns X20d24s and X20d38s hence fell out from this effort once the X12d pattern was defined. The X20d24s pattern maps 20 pairs and 24 single-ended pins from columns C and F to a single RT-2 connector. The X20d38s pattern maps 20 pairs and 38 single-ended pins from columns C and F over two RT-2 connectors. Note that the X20d38s pattern maps 78 pins to the RT-2 connector. This is the full complement of pins on the 114 pin XMC connector as the rest are dedicated to grounds.

VITA 46.9 speeds future development

By ensuring that mezzanine I/O differential pair mapping was defined in the VPX specification – and particularly VITA 46.9 – the VPX working group has ensured that mezzanine, basecard, and backplane/chassis designers will have the proper information to enable them to design interoperable PMC and XMC I/O mezzanine cards. This will help ease the adoption of new high-speed VPX and VPX-REDI applications, paving a smoother path to the future for the end users of today's challenging applications. **CS**



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