GUEST EDITORIALS

A clarification of the VME Renaissance

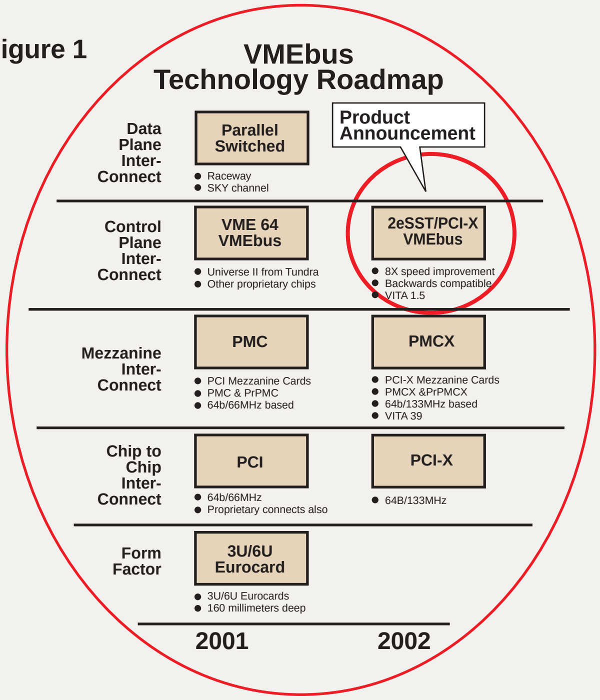
By Justin Moll

At the 2002 Bus & Board conference, Motorola Computer Group (MCG) announced the "VME Renaissance," celebrating 20 years of the VMEbus and outlining a roadmap for future VME developments. The presentation and subsequent articles have been intriguing and exciting to see. However, there was a subtle but important clarification that I would like to make.

First, I'd like to applaud MCG and the VME community for this effort. I personally was grossly misquoted in another publication as saying that I thought the VME Renaissance would fail. Quite the contrary, Bustronic and its parent company, Elma Electronic, have been staunch supporters of the VMEbus and very active in the VMEbus International Trade Association (VITA). We are excited to see a new era of innovation in the VME world and will continue to support these efforts. But, it is also important not to overlook another VME innovation, the VME320 backplane.

In MCG's Bus & Board presentation, their speaker said that "the VMEbus will be able to hit 320 Mbytes/sec in 2002." Further, the following chart was shown (see Figure 1), implying that the VMEbus would eventually reach 320 Mbytes/sec speeds sometime this year:

Figure 1



You could imagine our surprise as Bustronic has offered a VME backplane capable of 320 Mbytes/sec since 1997! As for the 2002 timeline, using General Micro Systems' OmniVME chip, the VME320 backplane was reportedly clocked at nearly 700 Mbytes/sec. (See Figure 2)

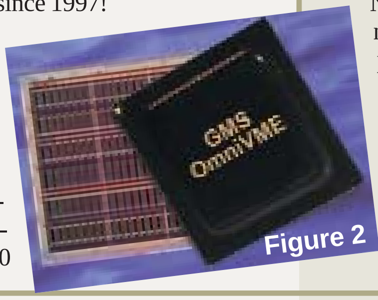


Figure 2

Clearly, the MCG speaker was discussing the standard VMEbus backplane when referring to "320

The vision of 2eSST

by Ben Sharfi

Motorola Computer Group (MCG) recently pre-announced a VMEbus chip that will implement the 2eSST protocol, enabling dramatically higher bandwidth for VMEbus systems. That protocol, however, has been fully defined for some time, and hardware supporting it has been on the market for nearly four years. The implementation of 2eSST in MCG's coming Tempe chip, due to start sampling in 3Q 2002, will rely on advanced high-power driver technology to achieve higher speeds, whereas the 2eSST-capable hardware already in the field relies on a simple but revolutionary backplane topology invented by Arizona Digital, known as VME320. Both approaches have their tradeoffs.

The nature of the Tempe approach is that it operates with legacy backplanes but requires new boards, while the VME320 requires new backplanes but accommodates legacy boards with small changes to the on-board protocols and FIFOs. The former is, thus, a good medium for conventional midlife upgrades to existing systems, whereas the latter, with far more performance headroom, is a bold new start. In any case, VME320 is technology agnostic: it can also take advantage of advances in bus driver silicon, and it has been applied to CompactPCI, PCI, and proprietary bus architectures in addition to VME. In both 2eSST approaches, OEMs may choose to support legacy transfer modes so that 2eSST-capable boards will be able to communicate with conventional boards at their more modest transfer rates.

The roots of 2eSST go back to the early 1990s, with the first of a string of midlife kickers for VME that would ultimately expand the 40 Mbyte/sec frontier of the 1980s to the 320 Mbyte/sec and faster realm today. Around the turn of the decade, a technique that was to become known as VME64 doubled the theoretical maximum VMEbus performance from 40 Mbytes/sec to 80 Mbytes/sec without challenging the technology of the day.

The brainchild of Performance Technologies, VME64 multiplexes 32 bits of data onto VME's previously unmultiplexed address bus, effectively turning it into a 64-bit bus. Subsequent VMEbus performance enhancements have all built on top of VME64, but the mindset of the time was that VME would probably always remain a 10 MHz bus.

Other, more technically challenging midlife kickers were explored, aired and, in some cases, implemented in the mid to late 1990s. A suite of VMEbus extensions called VME64x, for example, included a 2-edge (2e) transmission technique that effectively doubled theoretical data rates to 160 Mbytes/sec. Unfortunately, making VME64x work required special ETL drivers that were available from only a single supplier. Only one company implemented a product using VME64x.

Not included in the VME64x document was a source-synchronous overlay on the asychronous VMEbus, which had yet to be proven reliable using the bus drivers of the day. A source-synchronous transfer (SST) protocol operates without the traditional transfer-by-transfer acknowledgement cycles of VME, clocking (strobing) data across the bus as fast as the sender and receiver can manage it. The premise here was to raise the 40 Mbyte/sec theoretical (25 Mbyte/sec actual) data rate to a 160 Mbyte/sec actual data rate and, in conjunction with 2e, double VMEbus bandwidth once

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A clarification of the VME Renaissance (continued)

Mbytes/sec in 2002." If the presentation would have instead stated, "Using the 2eSST protocol, MCG's Tempe chip will allow standard VME backplanes to reach 320 Mbytes/sec speeds in 2002," that would have been more accurate and clear. However, to imply that VME will reach 320 Mbytes/sec in 2002 is a bit misleading. (No doubt this was unintentional and just an honest oversight.)

It is a fine point I am arguing, true. But, it's also true that the industry should know about VMEbus innovations that go far beyond standard backplane speeds. If we are celebrating innovation as an industry, let's proudly display some of our finest ideas.

Granted, the VME320 backplane has not seen the massive widespread acceptance of standard VME backplanes. However, it is a high-performance niche product that has been implemented in many military and commercial applications, and it continues to be an upgrade path for a variety of VME-based applications.

What is VME320?

The VME320, designed by Drew Berding of Arizona Digital in cooperation with Bustronic, is essentially a standard 6U VME64x backplane with remarkable routing topology. (See Figure 3) Unlike conventional backplanes that are limited by transmission line effects, such as reflections, VME320 backplanes act as lumped capacitances. The backplane provides clean monotonic waveforms suitable for very high-speed operation using the Two Edge Source Synchronous Transfer (2eSST) protocol. In a standard VME backplane, the signal routes are wired from slot to slot with a terminating resistor network at each end of the bus. The distributed inductance and capacitance of a fully loaded bus acts like a low-impedance transmission line. Line drivers cannot match the low impedance of the transmission line, and ringing and reflections increase with the data rate. In the VME320, a signal driven from slot 1 goes to slot 11 and then radiates out to all other slots. All the capacitance concentrates at slot 11 instead of having a transmission-line effect like conventional shared-bus backplanes. The result is that the equivalent circuit of the backplane is a simple lumped 200pF capacitance. In a standard VME backplane, the signals have propagation delay and must wait for their turn to go across the bus. Since the slots have their own paths in the VME320, the signals get to their destination several times faster. In fact, the VME320 can achieve 528 Mbytes/sec at 66 MHz with up to 21 slots (or over 1 Gbyte/sec at 133 MHz with 10 slots). This is 12 to 25 times the bandwidth of the original VME specification! This gives a huge performance upgrade potential to any system using VME backplanes without incurring any additional cost.

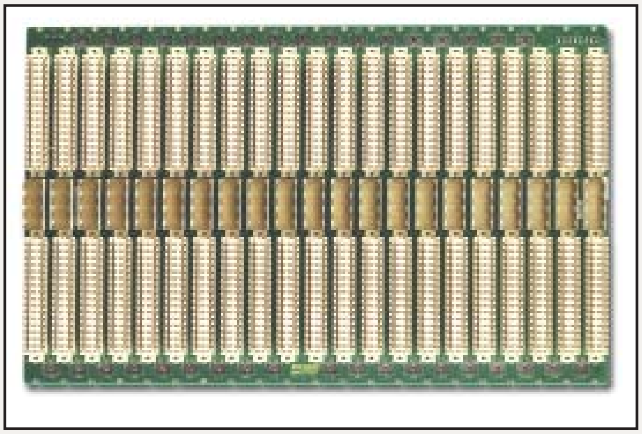

Figure 3. The VME320 may look like a standard VME64x backplane, but it offers superior performance and is backwards compatible to legacy VME/VME64x hardware and software.

The VME320 is fully backward compatible with VME64X and VME legacy hardware and software. The backplane meets and exceeds ANSI/VITA 1-1994 and IEEE P1014 specifications and the ANSI/VITA 1.1-1997, VME extensions standard. The VME320 backplane gives customers a dramatic backplane performance upgrade path, allowing them to simply plug in new cards that support the 2eSST protocol in addition to the standard VME protocol. The existing cards and the new cards coexist with no interoperability problems

We don't expect the VME320 to be the de facto replacement for current VME systems. But it continues to be an upgrade offering for systems demanding top performance. Bustronic, Elma Electronic, MCG, and dozens of other companies in the VME community will continue to advance VMEbus systems. We're making great progress in VITA on next-generation standards like VITA34 and have some exciting new concepts like the VXS backplane. As we take this important step into a new era of technology, let's be proud of all VME innovations. Whether large or small, mainstream or niche, open or proprietary, there are excellent VME technology developments that deserve our recognition. Let's keep them coming!

If you would like to learn more about the VME320, visit www.bustronic.com, www.nextgenbackplanes.com, or www.arizonadigital.com.

***Justin Moll** has over eight years of high-tech marketing and sales experience and has been the marketing manager for Bustronic since 2000. Also in charge of strategic marketing, Justin has helped establish partnerships with switch fabric silicon companies such as StarGen and PLX Technologies. His previous positions include marketing services manager for E21 Corporation and account manager for Elcon Products International, now a Tyco Electronics company. Justin received a BS in Business Administration from the University of California, Riverside.*

For more information, contact:

Bustronic
44350 Grimmer Blvd.
Fremont, CA 94538
Tel: 510-490-7388
Fax: 510-490-1853
Email: info@bustronic.com
Web site: www.bustronic.com

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again to 320 Mbytes/sec. Going synchronous, though, requires a clean and predictable electrical environment.

Getting to 320 Mbytes/sec

In January of 1997, Drew Berding, president of Arizona Digital Inc. and consultant to Bustronic Corporation, announced his revolutionary star-backplane scheme to the VSO. In March, he followed that with a press conference revealing the technical details of VME320. At the time, Ray Alderman, executive director of the VMEbus International Trade Association (VITA), dubbed VME320 "our silver bullet" against encroachments by CompactPCI. "Once again, we'll be the fastest bus in the business," he said.

The magic of VME320, as Berding sees things, is the use of simple synchronous protocols, which the predictable electrical environment provided by VME320 enables. "You can't run synchronous protocols on normal backplanes because that requires incident wave switching," Berding explained. But in VME, a single pulse from a TTL driver is not sufficient to drive a signal through transition; in fact, the system relies on subsequent signal reflections on the backplane.

"Eventually, things will rattle around enough times so you get up to a full signal swing," Berding explained, "but meanwhile you may go to switching threshold and hang there or even rattle back and forth through the threshold several times. That's totally impossible to work with in synchronous protocols because you have to wait for things to quiet down."

A VMEbus trace behaves like a slow, heavily loaded, low-impedance transmission line. Conventional ways of overcoming this might include terminating the lines to eliminate reflections, tweaking transceivers to tolerate reflections, or boosting driver current. Tempe takes the third approach, which relies on a new derivative of the old ETL drivers defined by VITA 2.1 in conjunction with Texas Instruments. Unfortunately, this brute-force approach to driving a conventional VMEbus backplane is a noisy, high-heat, single-sourced solution that only works for certain backplanes, with specified restrictions on which slots the boards can be loaded into. There are no safety margins, and it has not yet been demonstrated.

The VME320 scheme, in contrast, addresses the problem by implementing a topology different from the traditional daisy-chained or "stitched" backplane topology, in which lines and their signals travel sequentially from Slot 1 to Slot 2 to Slot 3 and so on. With VME320, all lines are laid out in a star, radiating out from the middle or "common" slot (Slot 11 in a 21-slot backplane) to all the other slots in what are essentially point-to-point connections. This, in effect, "makes the backplane look like a lumped capacitance [at Slot 11] rather than a transmission line," said Berding, "so when you drive it, you wind up with monotonic wave forms that don't ring back and forth." Rather than solving the reflection problems caused by transmission lines, the VME320 eliminates the transmission lines altogether.

"My waveforms are textbook," Berding said, "and VME320 does not use any technology that is not readily available." VME320 backplanes are readily available from Bustronic at prices comparable to those of conventional VME backplanes. For those desiring to make their own backplanes, licenses can be purchased from Arizona Digital.

The VME320 was first announced at 40 MHz (320 Mbytes/sec), but Berding claims that 1 Gbyte/sec is not beyond reach, and he has continued to optimize the scheme and achieve higher rates. Bustronic announced volume availability of 40 MHz GigaStar backplanes in early 1998 and, shortly thereafter, Arizona Digital and Bustronic demonstrated 66.625 MHz operation (above 500 Mbytes/sec), achieved by fine-tuning the 320 Mbyte/sec implementation.

At the time, Berding noted several items that could limit the ultimate performance of VME320:

- Series inductance (L) from the furthest driver (including card stub and connector) to the common point
- Total net capacitance (C), which includes the net traces, connectors, stubs and transceivers
- Transient drive current of the drivers
- Driver skew
- Reflections on the electrically short traces.

In April 1999, Berding revealed the technology behind the tune-up and he had, again, addressed the issues in an unconventional way (U.S. Patent #5,930,119): by widening the longest traces to reduce L significantly (at the expense of a slight increase in total C) and by using a common region (slots 9 through 13 in a 21-slot backplane) to further reduce L and eliminate the need for extra copper layers.

At the 2000 Bus & Board conference, Arizona Digital and General Micro Systems (GMS) demonstrated a 21-slot VME320 system by using a preproduction version of General Micro Systems' OmniVME VME-to-PCI bus bridge chip. In the demo, a frame buffer board sustained burst transfers to a video board over a fully loaded 21-slot VME320 backplane at in excess of 528 Mbytes/sec using conventional drivers. GMS has been incorporating the OmniVME chip, which supports 2eSST transfer rates up to 533 Mbytes/sec, onto CPU boards since mid 2000.

Most recently, Berding demonstrated an 80 MHz (640 Mbyte/sec) VME320 system, and Arizona Digital and GMS are collaborating on a cost-reduced version of the OmniVME chip. The new "miniOmni" will not have all the bells and whistles of the Omni chip, but it will be much more affordable. The intent of the miniOmni chip is to help drive VME320 to de facto standard status. It is being implemented in a CPLD. GMS also plans to provide a complete hardware reference design, so VME320 becomes, as Berding put it, "a no-brainer drop-in solution."

With 320 Mbyte/sec and higher transfer rates here now, 533 Mbytes/sec in reach, and even higher rates on the near horizon, VMEbus becomes a far more capable platform for demanding high-end applications. The heavy traffic in leading-edge military and communications applications demand bandwidth, with their data hungry Fibre Channel and ATM controllers, banks of Fast Ethernet controllers, simulation-grade graphics, and huge amounts of multimedia data. As bandwidth demands grow even higher in the future, the "old" VMEbus will still be there to take care of the job.

__Benjamin K. Sharfi__ is the president and CEO of General Micro Systems, Inc., which he founded in 1979 with the goal of developing complete board level microprocessor products. Previously he worked for Metron Corporation and Rockwell International, where he was involved in microprocessor systems development. Sharfi is a current member of VITA and PICMG and was a member of IEEE for over 10 years. He received his BS in electrical engineering in 1976 from California Polytechnic College of Pomona.

For more information, contact:
General Micro Systems
8358 Maple Place • Rancho Cucamonga, CA 91729-3689
Tel: 909-980-4863
Web site: www.gms4sbc.com