Using PCI Express for next-generation battlefield applications

By Manville Chan and Steve Moore

PCI Express is set to make its mark in the military technology market. Key factors in its future growth in military applications include engineers' wide-ranging familiarity with it, its widespread use in commercial markets, and the military's need for virtually instant, high-volume data processing.

PCI Express, a high-speed peripheral interconnect bus, evolved from PCI and PCI-X and is widely used in computers, servers, and mobile devices. Established as a standard in 2001, PCI Express' commercial implementation reached the market in 2004. While PCI utilizes a bus-based architecture, PCI Express is built around a serial, point-to-point link between two devices that allow higher throughput (up to 80 Gbps) while reducing printed circuit board pin and trace counts to simplify hardware architecture. PCI Express maintains backward compatibility with PCI and PCI-X at the packet level, allowing existing PCI and PCI-X software code to be reused with PCI Express hardware.

PCI Express is widely used in the commercial marketplace where leading chip manufacturers such as Intel were early adopters. However, it hasn't significantly penetrated the military embedded systems market, which traditionally lags behind commercial technology adoption. Currently only a handful of vendors manufacture PCI Express compatible products for the military market, though companies such as Cornet Technology, Inc. and VMETRO are entering the market to fill military requirements. The benefits of PCI Express adoption by the military market include: the increasing number of engineers familiar with it, adoption by the commercial industry, and the need for nearly instantaneous high-volume data processing by the military.

The case for military PCI Express adoption

Since its acceptance as a standard in 2001, PCI Express has developed a high percentage of recognition by design engineers. According to a study conducted by a leading industry publication in July 2006, PCI Express received an 82.2 percent recognition rating among embedded engineers compared to 91.4 percent for PCI, 57.4 percent for InfiniBand, and 52.9 percent for Rapid I/O. [1]

The high number of engineers with knowledge of PCI Express, as well as its full compatibility with earlier standards such as PCI and PCIx, has been a factor in the accelerated adoption of PCI Express technology. This is important because in today's tight employment market, companies are concentrating on open standards with a large pool of knowledgeable engineers.

Industry support has been a catalyst for PCI Express adoption. With both VITA (www.vita.com) and PCI-SIG (www.pcisig.com) playing a crucial role in advocating the standard, there has been an increasing number of product support from silicon and board-level vendors (see Table 1 for vendor support listing). According to industry analyst firm Venture Development Corporation (VDC), PCI Express will account for 19 percent of the PMC/XMC I/O mezzanine card market in 2007 (or $53.6 million in shipments).

SWITCHED INTERCONNECT

The evolution of switched interconnect technology

Switched interconnect technology incorporates high-volume data and processing capabilities into a network. This technology enables embedded engineers to design highly scalable processing systems. In the mid to late 1990s, standards such as Skychannel (ANSI/VITA 10) and Raceway (ANSI/VITA 5.1) evolved to provide backplane switch interconnect technologies for the military embedded community.

INTERCONNECT TECHNOLOGIES CONVERGE

Converging peripheral interconnect and switched interconnect technologies

Being both a peripheral interconnect bus and a serial switched interconnect, PCI Express brings the best of both worlds to the embedded community. It is backward compatible with PCI and PCI-X, and yet enables a large number of devices to be interconnected in a cross-bar matrix switch.

PCI combines performance and scalability. Each lane of PCI Express consists of four wires – one differential pair simplex transmission channel in each direction. Each transmission channel runs at a baud rate of 2.5 Gbps. The number of lanes can be scaled to 2, 4, 8, 12, 16, and 32. With 32 lanes, PCI Express supports a transfer rate of 80 Gbps in each direction. The new PCI Express 2.0 specification proposed by PCI-SIG (www.pcisig.com) doubles the transfer rate to 160 Gbps for x32 lane. Conventional PCI at 133 MHz and 64 bits has a transfer rate of about 8 Gbps in a nearly 80-wire, bused, effectively simplex interface. PCI Express surpasses this performance with a 16-wire x4 link that can transfer a similar amount of data in each direction, with one-fifth the pin and trace resources.

The military embedded market, which needs almost instantaneous, high-volume data processing for applications such as aerial surveillance, is likely to begin adopting PCI Express as a natural progression from the COTS systems presently using PCI and PCI-X bus architecture. The recent VME renaissance effort specifically brings PCI Express to VME under the VME Switched Serial (VXS, VITA 41.4) and Serial Mezzanine Card (XMC, VITA 42.3) standards.

Table 1 compares various switched serial fabric and high-speed I/O interconnect technologies, including Aurora, GbE, 10 GbE, InfiniBand, PCI Express, Serial RapidIO, and StarFabric. PCI Express clearly leads other technologies in terms of the number of available component and board-level products and endorsements from various industry standard bodies.

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PCI Express for military applications

High-speed data sharing

Mission-critical military Signal Intelligence (SIGINT) applications can collect up to several gigabits of digitized raw data every second.

Fabric technology	Aurora	GbE	10 GbE	InfiniBand	PCI Express	Serial RapidIO	StarFabric
Standards org	Xilinx	IEEE	IEEE	InfiniBand TA	PCI-SIG	RapidIO TA	StarFabric TA
Current spec (date)	SP002 1.3 (June 2004)	IEEE 802.3ab (1999)	IEEE 802.3-2005	1.2 (Oct. 2004)	1.1 (March 2005)	1.3 (June 2005)	StarFabric proponent StarGen has changed strategic direction, leaving StarFabric's future unknown
Further specs (date)	VITA 41.5, VITA 42.5, VITA 55	AMC.2, PICMG 2.16, PICMG 3.1, VITA 41.3, VITA 46.6	VITA 46.7	PICMG 3.2, VITA 41.1, VITA 46.8	AMC.1, EXP.0, PICMG 3.4, VITA 41.4, VITA 42.3, VITA 46.4, COMe	AMC.4, PICMG 2.18, PICMG 3.5, VITA 41.2, VITA 42.2, VITA 46.3	PICMG 2.17 PICMG 3.3
Microstrip baud rate (Gbps/lane/direction = 4 wires)	1.25/2.5/3.125	1	3.125	2.5/5/10	2.5 (Gen 1)/ 5.0 (Gen 2)	1.25/2.5/3.125	0.622
Target applications	FPGA interconnect	Networking, medium-speed I/O	Networking, high-speed I/O	Server interconnect for high-end clustered computing	High-speed I/O and chip-to-chip communication	DSP/CPU inter-communication and backplane interconnect	Medium-speed chip-, module-, and system-level interconnect
Major component support	Xilinx	Many	Fulcrum Microsystems, Broadcom, Vitesse, Marvell	Mellanox	PLX Technology, Intel, StarGen, Tundra, IDT, AMCC, Freescale, TI, Marvell, Broadcom	Tundra, Freescale, TI	StarGen
VME board-level vendors	VMETRO, Pentek, 4DSP, TEK Microsystems, Micro Memory, Nallatech, GE Fanuc	Many	Evolving Technology	GE Fanuc	Cornet Technology, VMETRO, TEK Microsystems, RECAB, Mercury Computer, GE Fanuc, Curtiss-Wright	Mercury Computer, Micro Memory, VMETRO, Pentek	Curtiss-Wright, GE Fanuc, Micro Memory
Advantages	Lightweight protocol, high speed	Well-known, safe technology	Built upon ubiquitous GbE	High data rates	Legacy software compatibility, fairly low header processing O/H	Simplicity and low O/H, intra- and interchassis suitability, more flexible topology	Backwards compatible to PCI (address method)
Disadvantages	Not a switched fabric, no silicon outside of FPGAs	High overhead for header processing, no QoS standard	High overhead for header processing, no auto-negotiation down to slower speeds	S/W complexity, limited ecosystem support	Difficult to implement large arrays	No path from legacy systems/code, smaller support group due to lack of interest from PC market, minimal chip-level support	Low speed

Table 1

This data must be piped into a processing engine in real time, and the processed data must be disseminated similarly. PCI Express is ideal for this type of high-speed data transfer application.

Real-time data analysis and dissemination in a net-centric military system

Real-time data analysis and dissemination are increasingly important to military and other intelligence operations. For example, terrorists often place their operations in highly populated civilian areas. To discover these sites, the military uses Unmanned Aerial Vehicles (UAVs) to capture photographs, infrared, and electronic signatures, which are then analyzed to pinpoint the location of the enemy. Once a target is defined, the UAV relays signal to ground-based missile launchers. Accurate and timely data imagery and analysis are crucial to a successful operation. If image-processing techniques are not sufficiently "intelligent," an operation could potentially misinterpret a civilian site for a military position. In addition, if the information is not disseminated in real time, the enemy's military operations could shift, closing the strike window.

As a high-speed interconnect technology, PCI Express supports the channeling of information at a high rate to processing elements. Many of the new, high-speed data acquisition I/O cards utilize PCI Express to enhance throughput. When processing video images or other complicated data in real time, the amount of transmitted data can be significant. The ability to process this type of information is often limited by how quickly it can stream into the compute elements. In such a scenario, PCI Express provides a measurable difference in the ability to utilize data quickly and efficiently.

The advent of network-centric warfare initiatives such as the Joint Tactical Radio System (JTRS) plays a crucial role in technological decisions made by military embedded designers. JTRS fosters intelligence sharing among a wide range of military equipment and data centers in government agencies. This enables cross-analysis of data so that the military can identity an enemy more accurately and precisely in a critical combat environment. Network-centric warfare requires intelligence to be stored and retrieved to/from a massive cross-analysis data repository. By using PCI Express, an embedded subsystem can be linked to other servers in which PCI Express has already been widely used.

In a SIGINT system (Figure 1) PCI Express can greatly enhance information processing in the system using high-speed, full-duplex links. These links operate at a rate of 10 Gbps (2.5 Gbps x 4) in each direction. RF antenna signals are digitalized using a PCI Express VXS digitizer. The digitizer is linked through a meshed configuration to a VXS multiprocessing computer. The multiprocessing computer system includes two PCI Express XMC sites, allowing processed data to be sent to a data repository via Serial FPDP.

PCI Express: the future of military embedded applications

Deployment of PCI Express technology in high-performance, real-time battlefield applications offers the military a number of benefits. These include reduced wire count complexity via using a serial versus parallel interconnect, a wide selection of component vendors, and access to a large pool of knowledgeable PCI-experienced engineers. Since PCI Express is widely used in database server applications, an embedded PCI Express system can be integrated into an IT infrastructure in a network-centric warfare environment, permitting disparate systems to communicate with one another. As an open standard technology that is fast, scalable, and backward-compatible, PCI Express is expected to make significant in-roads to military embedded applications in the next few years. **CS**

Reference

1. See EE Times survey: http://www.eetimes.com/news/latest/showArticle.jhtml?articleID=190400383

A SIGINT Application using PCI Express Under a Meshed VXS System

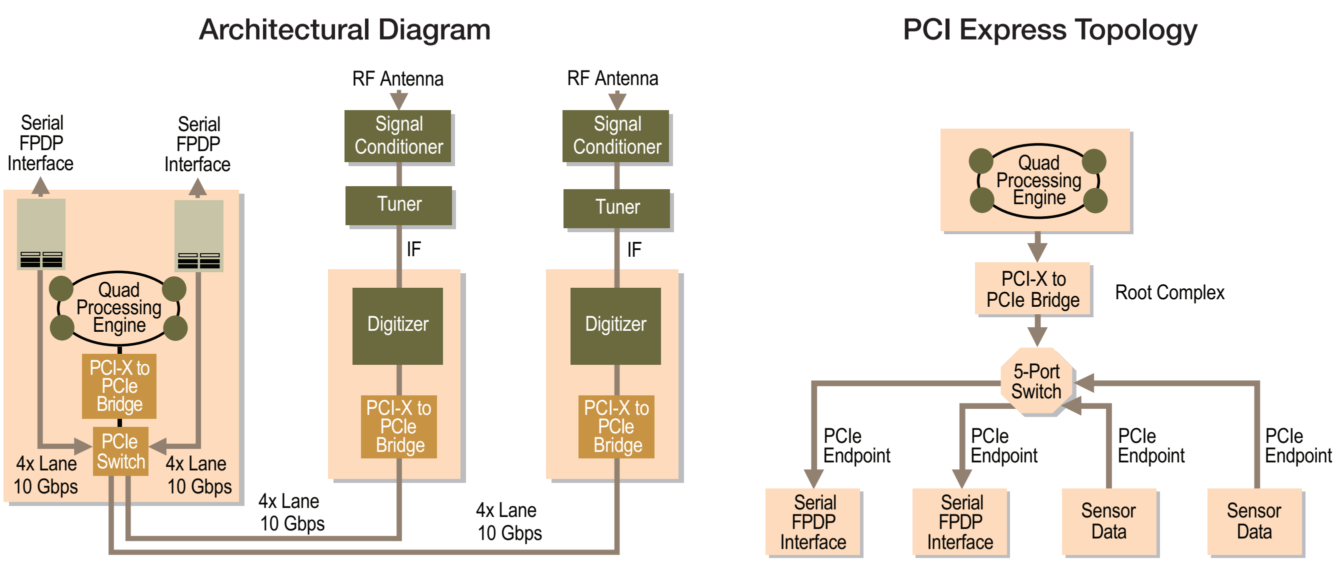

Figure 1

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